

# Enrico/Caruso 15" UMA Schematics Document

## Sandy Bridge

Intel PCH

2011-06-02

REV : A00



DV15 HR Vos GIGA HDMI NoSurge



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size  
A3

Document Number

**Enrico/Caruso 15 HR**

Rev

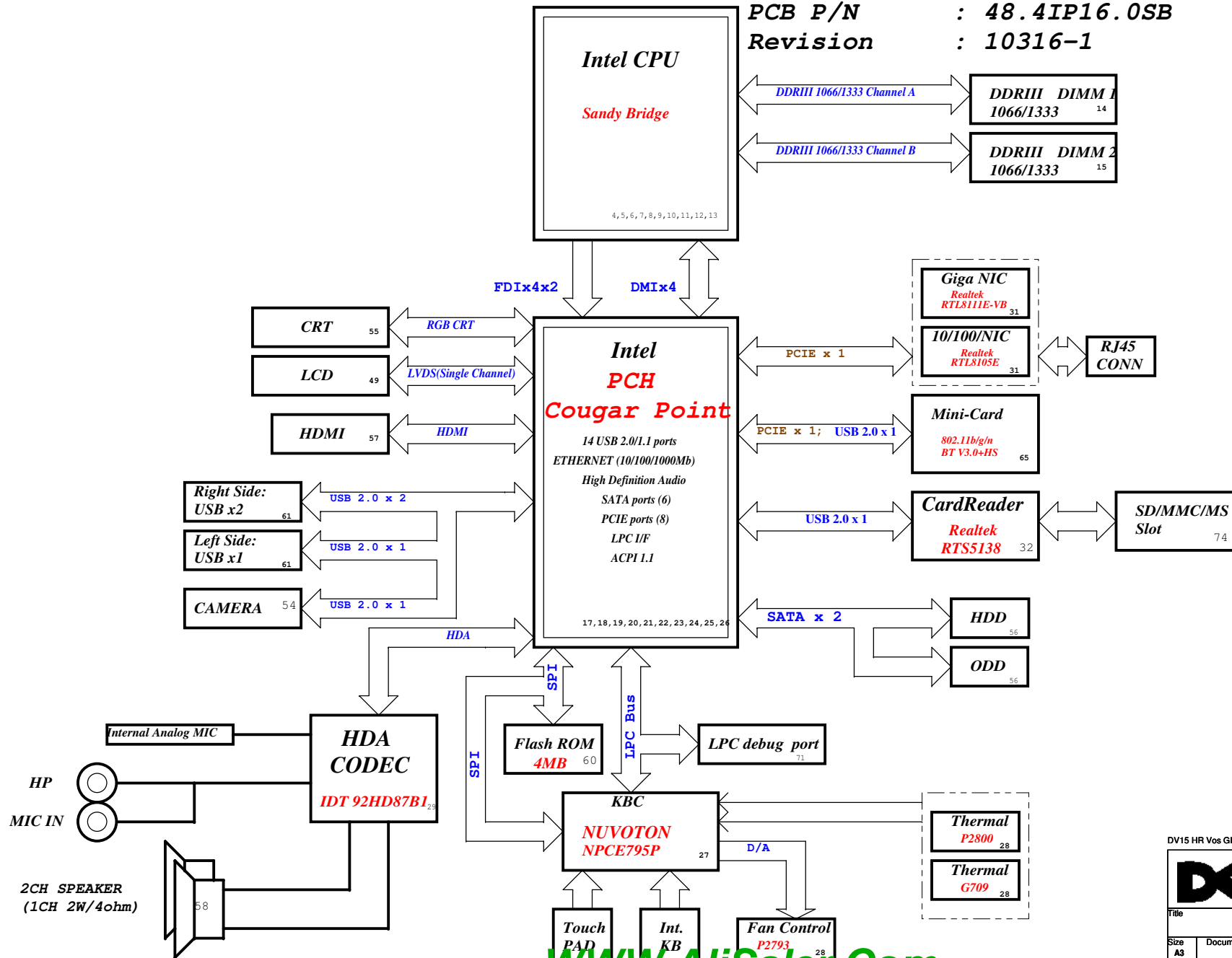
**X01**

Date: Thursday, June 02, 2011

Sheet 1 of 104

# DV15 Huron River UMA Block Diagram

Project code : 91.4IP01.001  
PCB P/N : 48.4IP16.0SB  
Revision : 10316-1



SYSTEM DC/DC	
TPS51461	48
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0
CPU DC/DC	
ISL95831HRTZ	42~44
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
GFX DC/DC	
ISL95831HRTZ	44
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE
SYSTEM DC/DC	
TPS51218	45
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
TPS51123RGER	41
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5
SYSTEM DC/DC	
TPS51216RUKR	46
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3
MAXIM CHARGER	
BQ24707	40
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT
SYSTEM DC/DC	
TPS51311RGTR	47
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0
Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0
PCB LAYER	
L1:Top	L4:Signal
L2:GND	L5:VCC
L3:Signal	L6:Bottom

Huron River Schematic Checklist Rev.0_7	
Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> <b>No Reboot Mode with TCO Disabled:</b>
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. <b>Disable Danbury:</b> left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] <b>Disable Danbury:</b> leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

## USB Table

## PCIE Routing

LANE1	X
LANE2	Onboard LAN
LANE3	x
LANE4	Mini Card1 (WLAN)
LANE5	X
LANE6	X
LANE7	X
LANE8	X

## SATA Table

SATA	
Pair	Device
0	HDD1
1	X
2	X
3	X
4	ODD1
5	X

Pair	Device
0	X
1	USB Ext. port 1
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

Huron River Schematic Checklist Rev.0_7			
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	<b>PCI-Express Static Lane Reversal</b>	<b>1:</b> Normal Operation. <b>0:</b> Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		<b>Disabled</b> - No Physical Display Port attached to Embedded DisplayPort. <b>0:</b> Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	<b>PCI-Express Port Bifurcation Straps</b>	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	<b>PEG DEFER TRAINING</b>	<b>1:</b> PEG Train immediately following xxRESETB de assertion <b>0:</b> PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC GFXCORE	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-12.6V 9V-19V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_IAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

## SMBus ADDRESSES

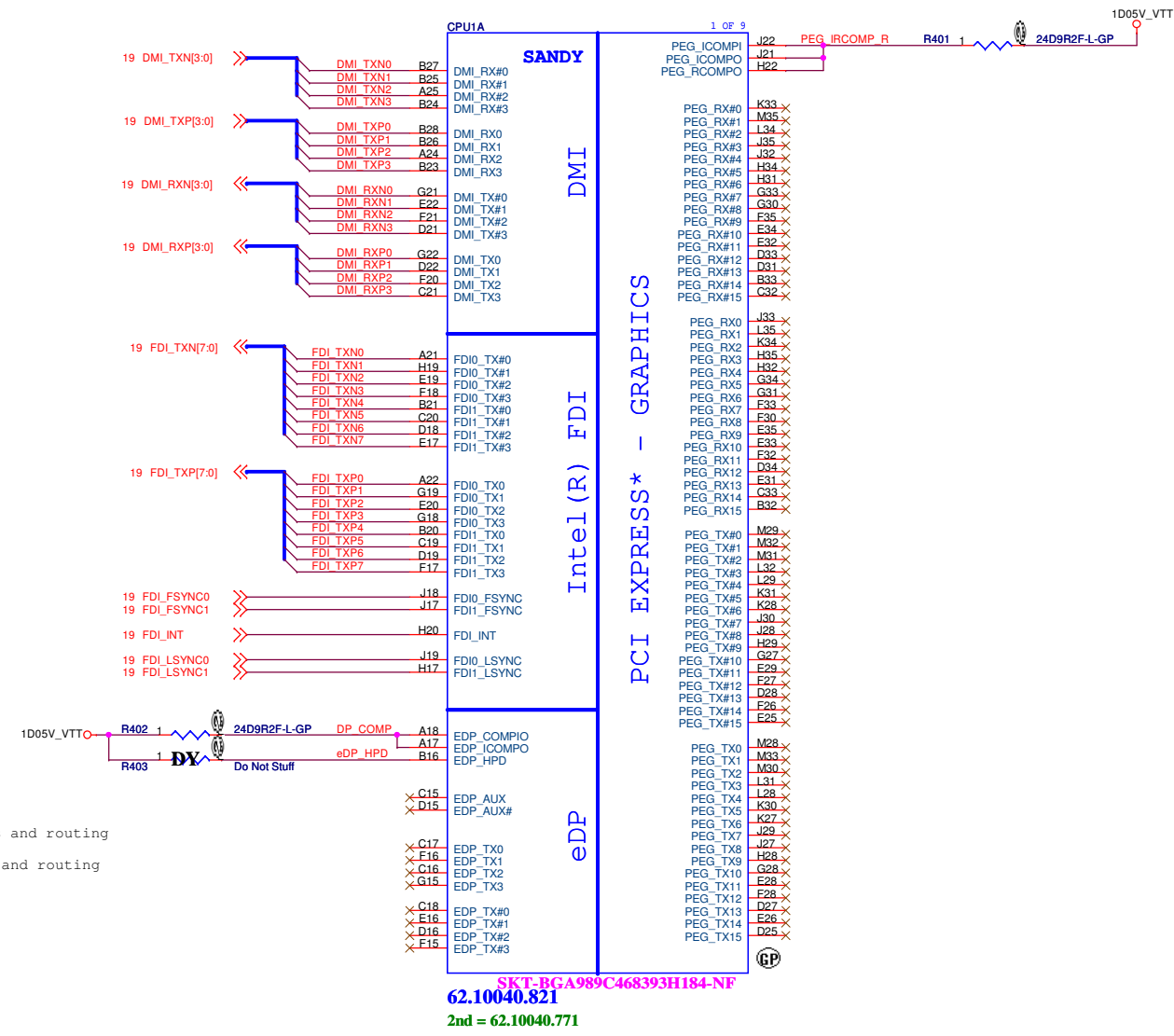
I <sup>2</sup> C / SMBus Addresses		HURON RIVER ORB		
Device	Ref Des	Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

OV15 HR Vos GIGA HDMI NoSurge

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Title			
<b><i>Table of Content</i></b>			
Size A3	Document Number	<b>Enrico/Caruso 15 HR</b>	Rev <b>X01</b>
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SSID = CPU

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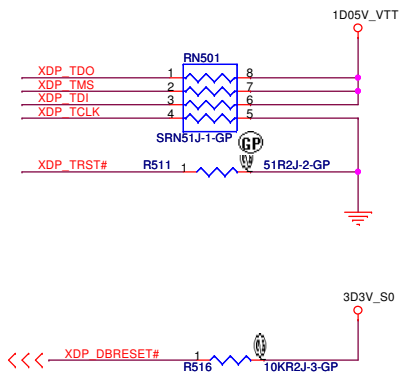
**DELL**

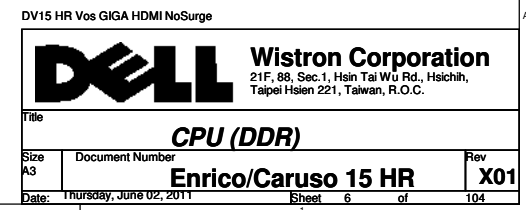
**CPU (PCIE/DMI/FDI)**

Size A3 Document Number Enrico/Caruso 15 HR Rev X01

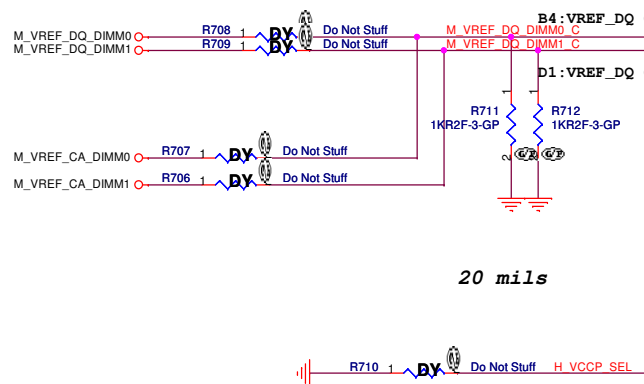
Date: Thursday, June 02, 2011 Sheet 4 of 104

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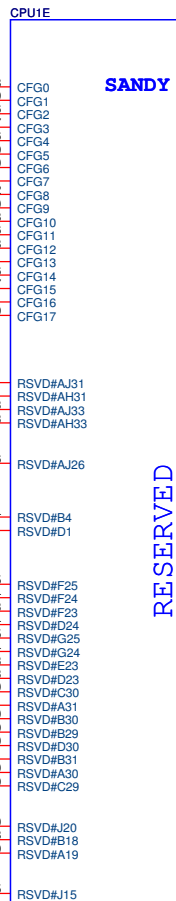




### M3 - Processor Generated SO-DIMM VREF\_DQ



20 mils



SKT-BGA989C468393H184-NF  
62.10040.821  
2nd = 62.10040.771

#### PEG Static Lane Reversal

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
------	--

#### Display Port Presence Strap

CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port
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#### PCIe Port Bifurcation Straps

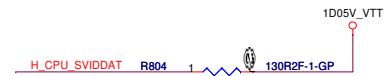
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled
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#### PEG DEFER TRAINING

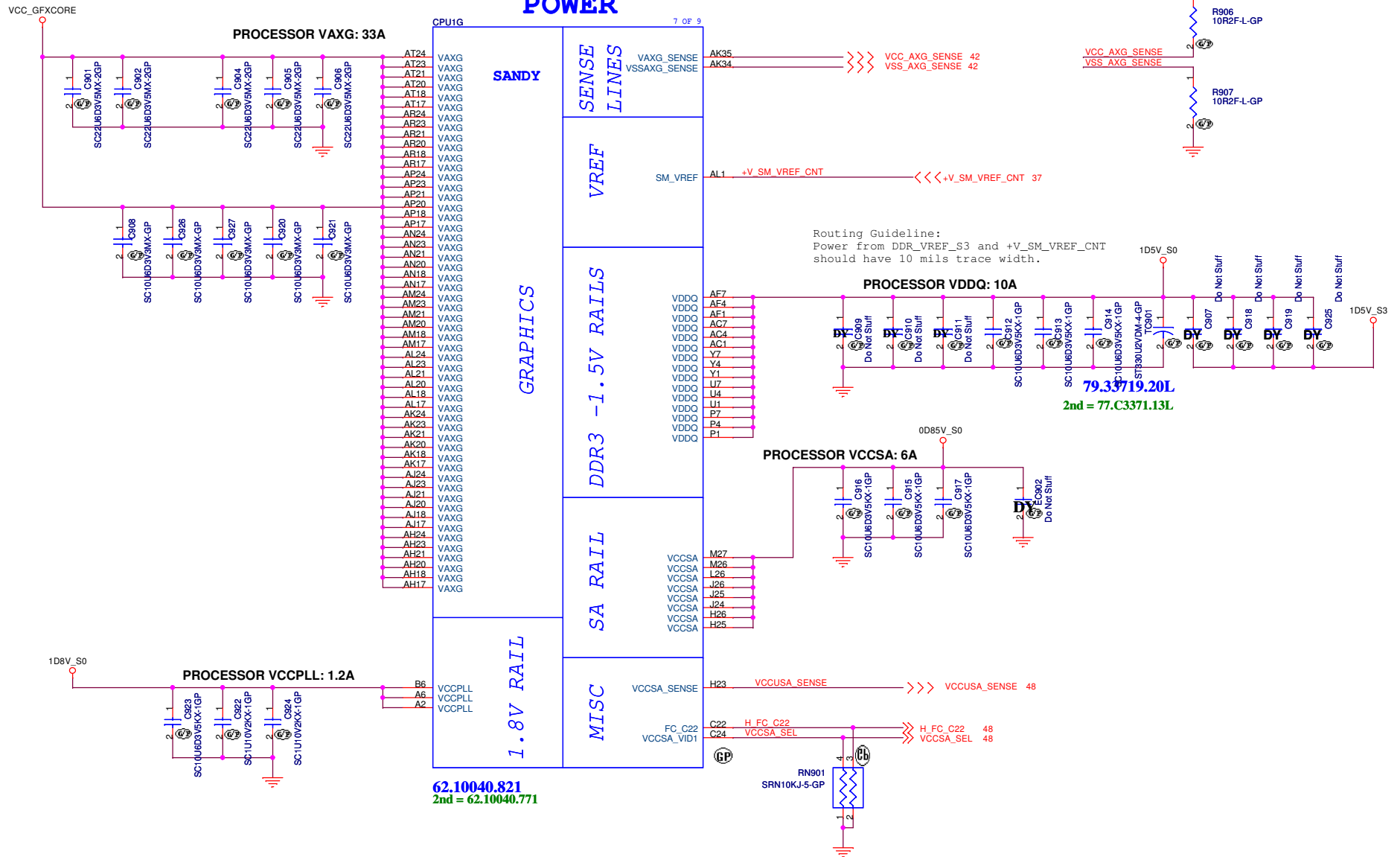
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
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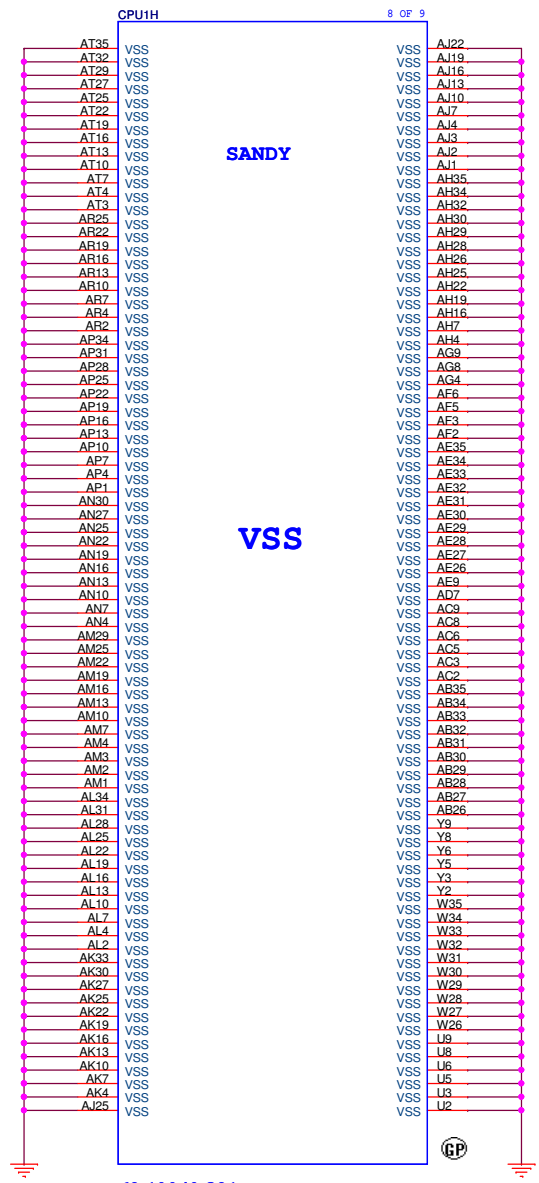
DV15 HR Vos GIGA HDMI NoSurge

<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: <b>CPU (RESERVED)</b>			
Size: A3	Document Number: <b>Enrico/Caruso 15 HR</b>	Rev: <b>X01</b>	
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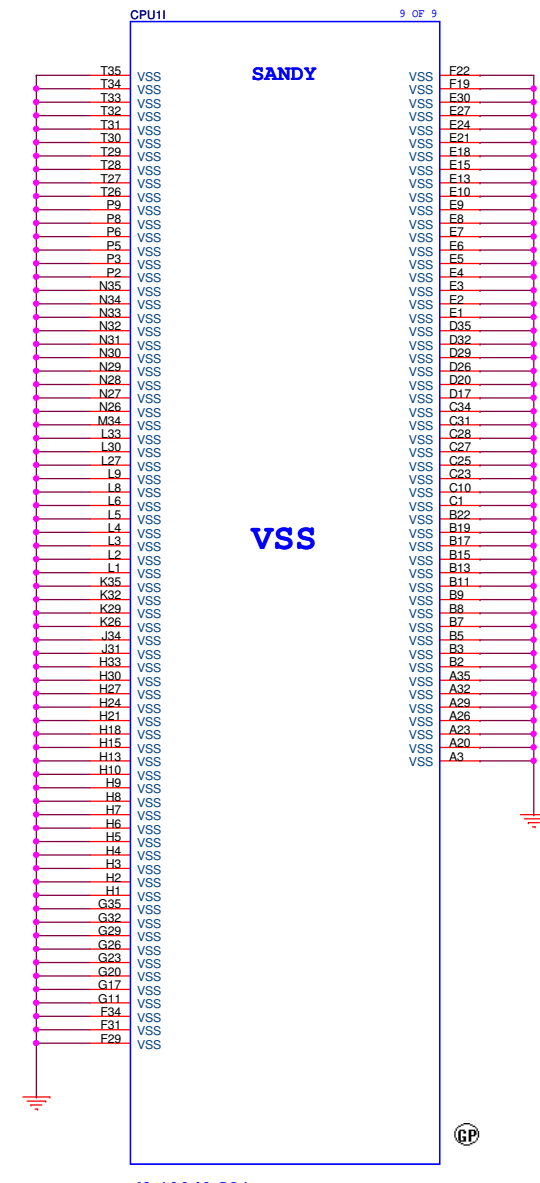




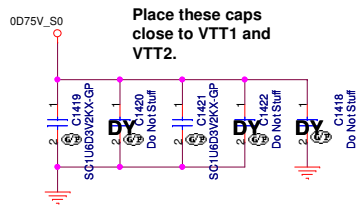




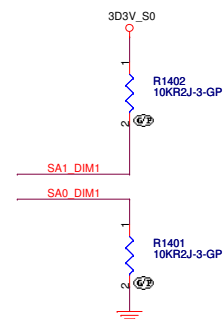
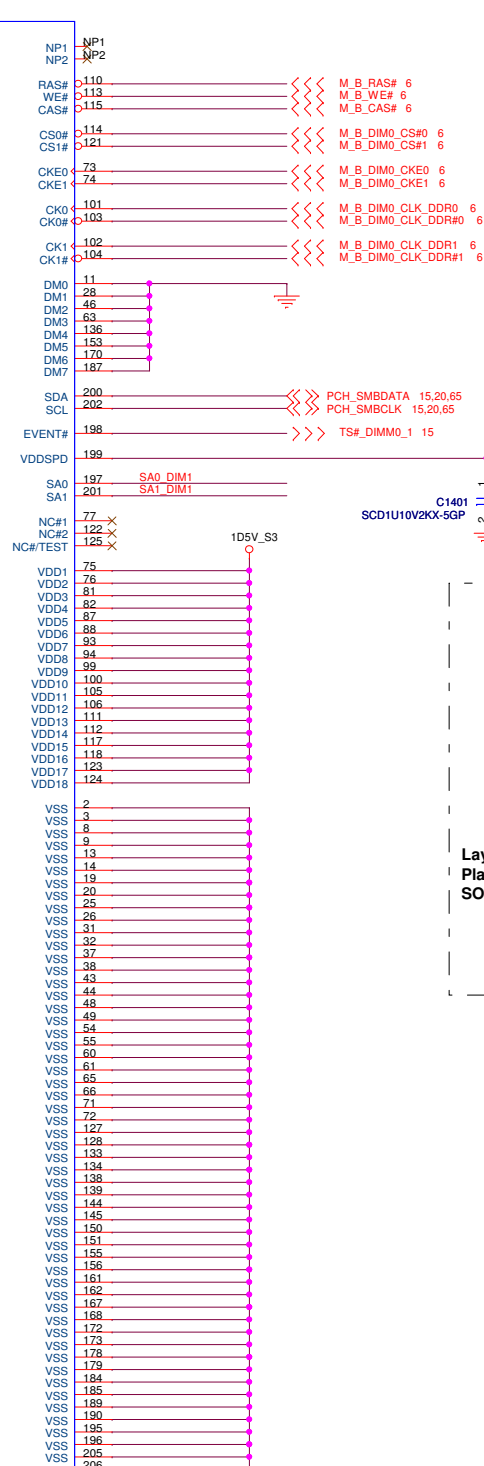
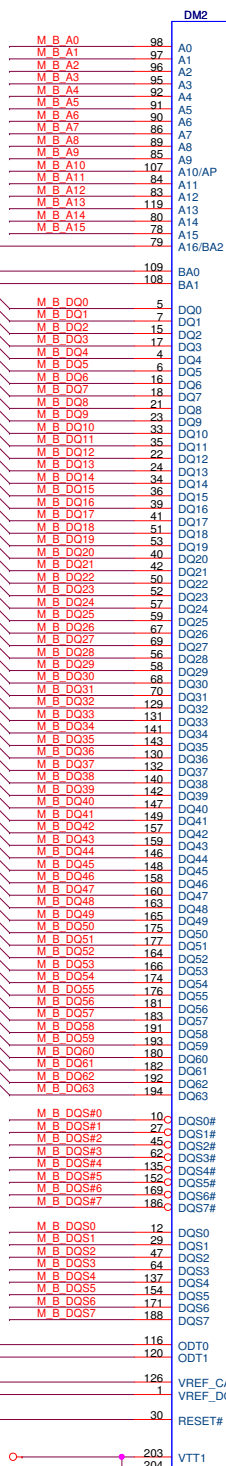
62.10040.821  
2nd = 62.10040.771



62.10040.821  
2nd = 62.10040.771

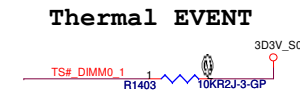


**Place these caps  
close to VTT1 and  
VTT2.**

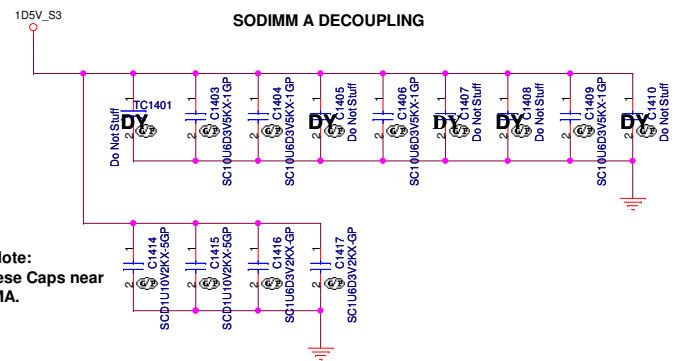


**Note:**  
If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30

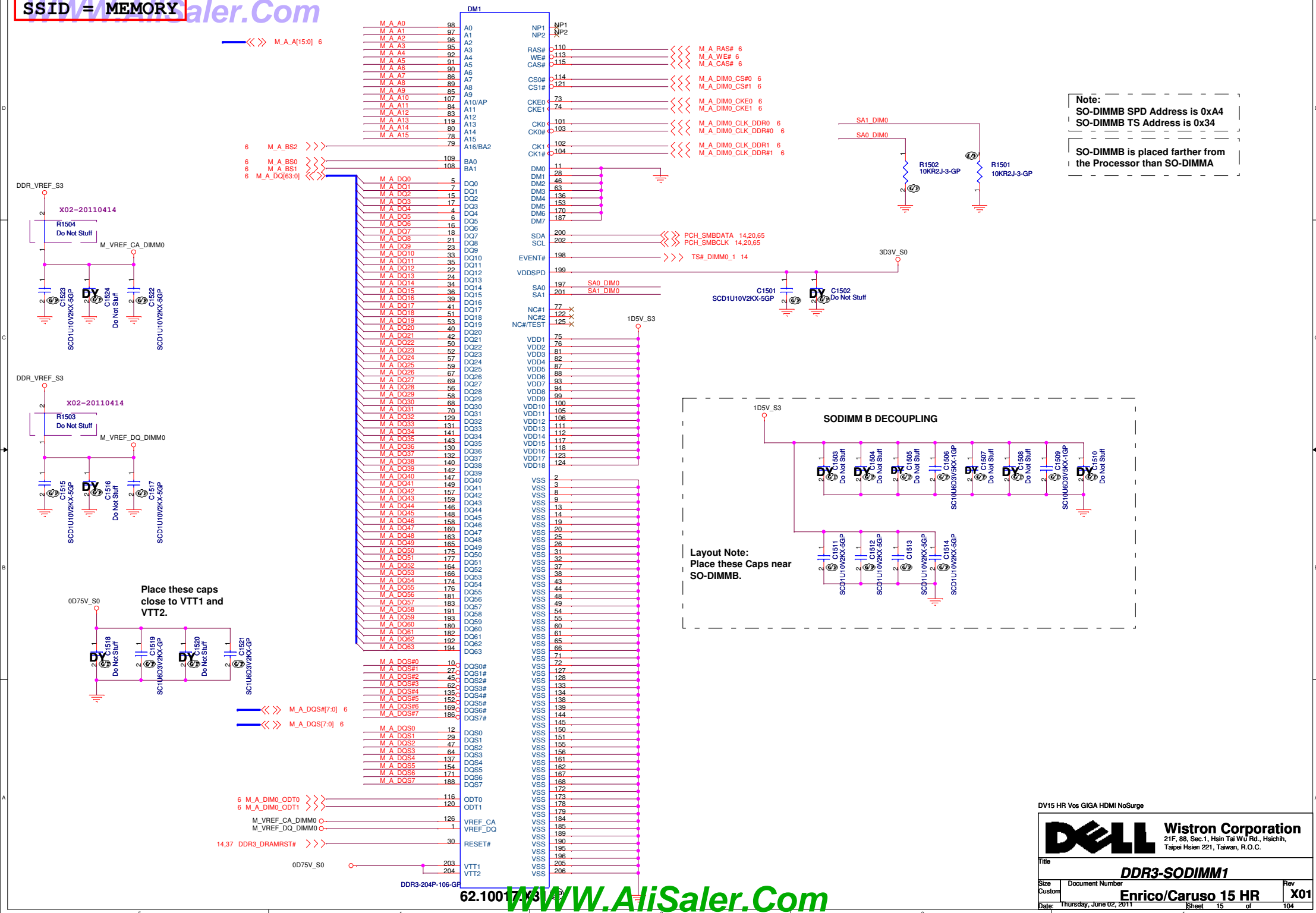
If SA0\_DIM0 = 0, SA1\_DIM0 = 1  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32

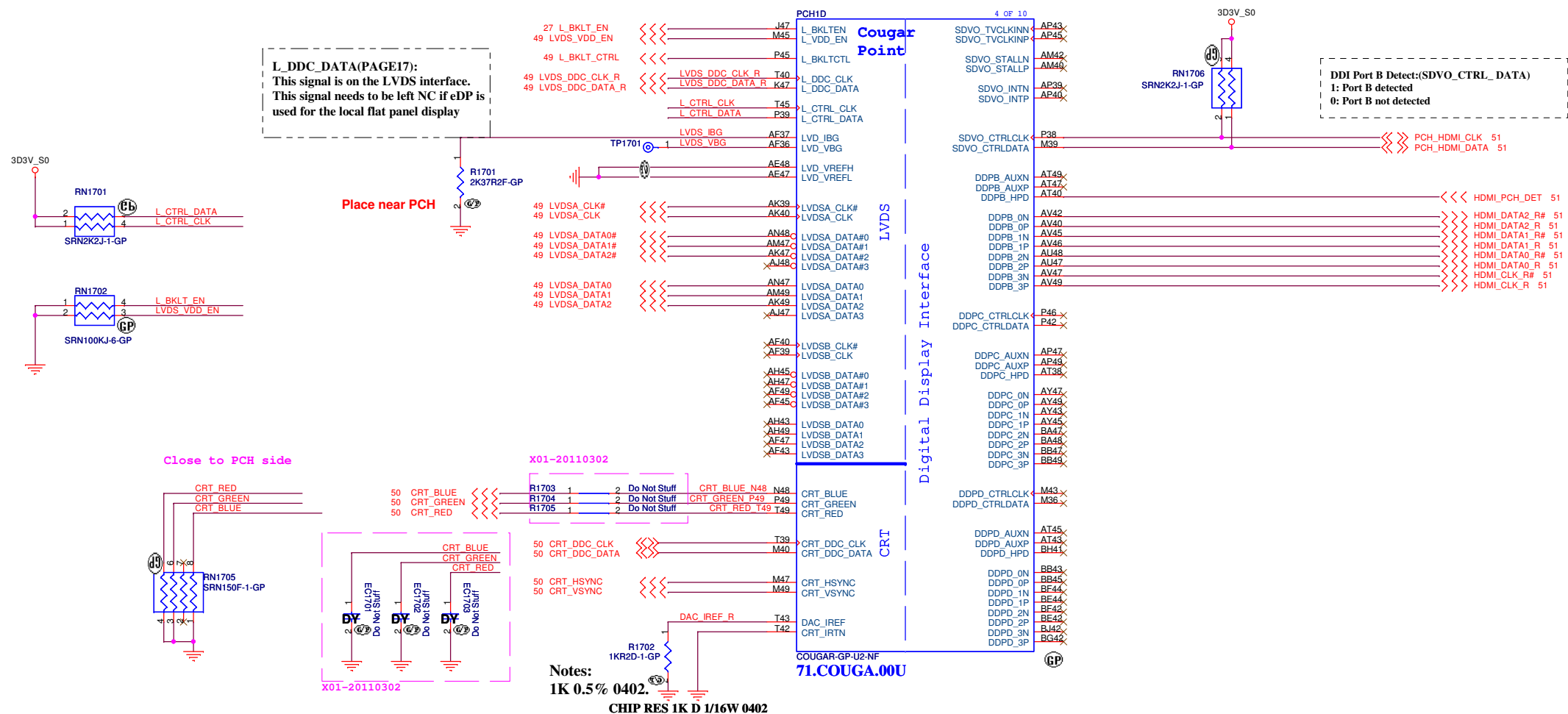


## Thermal EVENT



**Layout Note:**  
Place these Caps near  
SO-DIMMA.





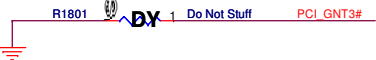
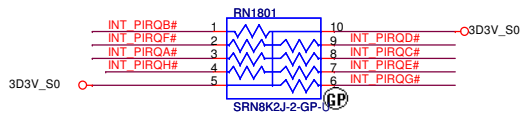
DV15 HR Vos GIGA HDMI NoSurge



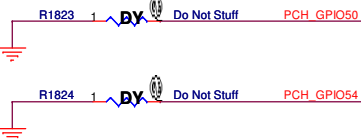
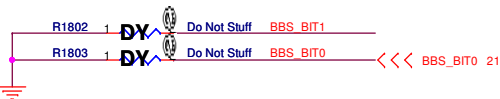
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Title			<b>PCH (LVDS/CRT/DDI)</b>	
Size A3	Document Number	<b>Enrico/Caruso 15 HR</b>		Rev <b>X01</b>
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SSID = PCH



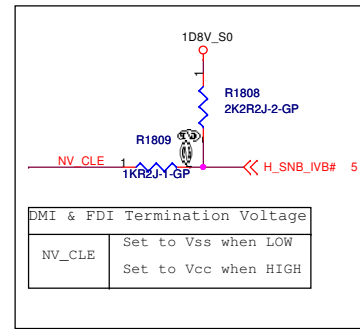
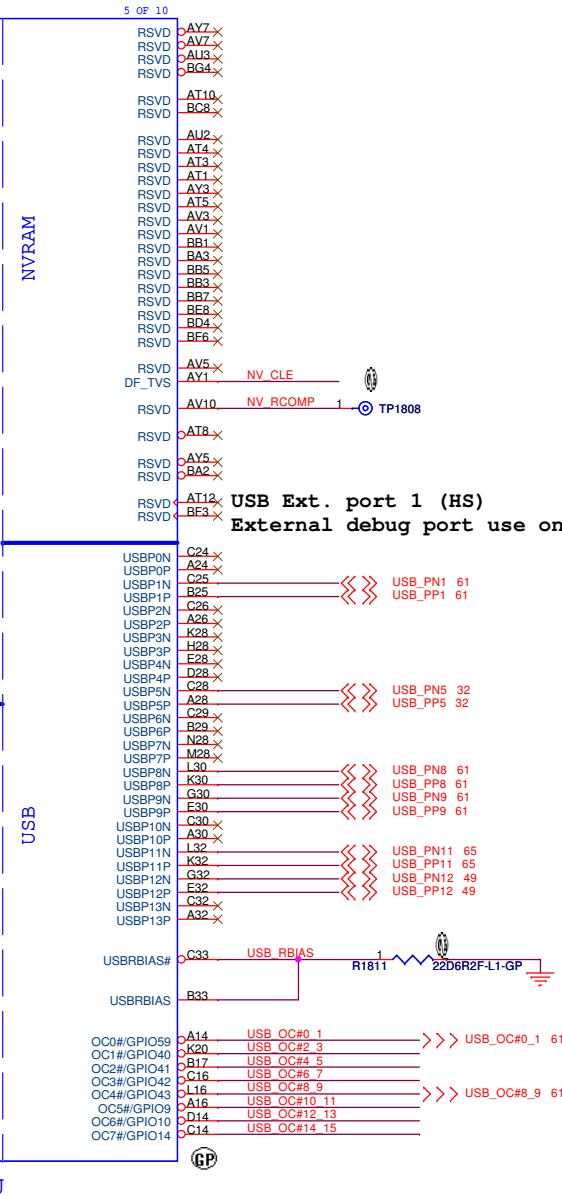
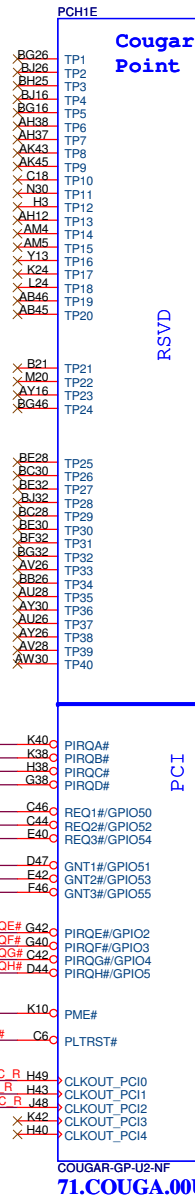
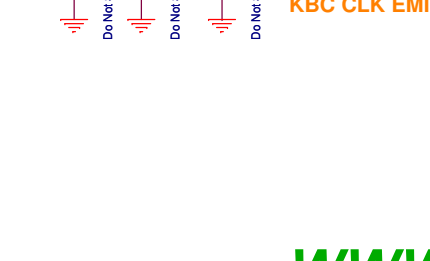
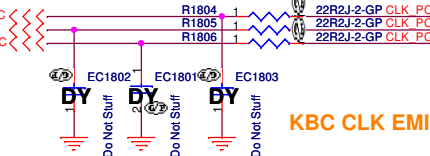
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

56 SATA\_ODD\_DA# >>> R1813 1 2 Do Not Stuff

TP1806 1 PCI PME# K10  
TP1801 1 PCI PLTRST# C6



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

USB Ext. port 1 (HS)  
External debug port use on Huron river platform  
**USB Table**

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

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**DELL**

Title: **PCH (PCI/USB/NVRAM)**

Size A3 Document Number: **Enrico/Caruso 15 HR** Rev: **X01**

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SSID = PCH

4 DMI\_RXN[3:0]  
4 DMI\_RXP[3:0]  
4 DMI\_TXN[3:0]  
4 DMI\_TXP[3:0]

FDI\_TXN[7:0] 4  
FDI\_TXP[7:0] 4

Signal Routing Guideline:  
DMI\_ZCOMP keep W=4 mils and  
routing length less than 500  
mils.  
DMI\_IRCOMP keep W=4 mils and  
routing length less than 500  
mils.

4 DMI\_RXN0  
4 DMI\_RXN1  
4 DMI\_RXN2  
4 DMI\_RXN3  
4 DMI\_RXP0  
4 DMI\_RXP1  
4 DMI\_RXP2  
4 DMI\_RXP3  
4 DMI\_TXN0  
4 DMI\_TXN1  
4 DMI\_TXN2  
4 DMI\_TXN3  
4 DMI\_TXP0  
4 DMI\_TXP1  
4 DMI\_TXP2  
4 DMI\_TXP3

BC24  
BE20  
BG18  
BG20  
BE24  
BC20  
BJ18  
BJ20  
AW24  
AW20  
BB18  
AV18  
AY24  
AY20  
AY18  
AU18

PCH1C

3 OF 10

Cougar  
Point

DMI

FDI

FDI\_RXN0  
FDI\_RXN1  
FDI\_RXN2  
FDI\_RXN3  
FDI\_RXN4  
FDI\_RXN5  
FDI\_RXN6  
FDI\_RXN7

FDI\_RXP0  
FDI\_RXP1  
FDI\_RXP2  
FDI\_RXP3  
FDI\_RXP4  
FDI\_RXP5  
FDI\_RXP6  
FDI\_RXP7

FDI\_INT

FDI\_FSYNC0

FDI\_FSYNC1

FDI\_LSYNC0

FDI\_LSYNC1

DSWVRMEN

DPWROK

WAKE#

CLKRUN#/GPIO32

SUS\_STAT#/GPIO61

SUSCLK#/GPIO62

SLP\_S5#/GPIO63

SLP\_S4#

SLP\_S3#

SLP\_A#

SLP\_SUS#

PMSYNCH

SLP\_LAN#/GPIO29

GP

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1D05V\_VTT

R1901

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750R2F-GP

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100KR2J-1-GP

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100KR2J-1-GP

49D9R2F-GP

750R2F-GP

100KR2J-1-GP

100KR2J-1-GP

100KR2J-1-GP

100KR2J-1-GP

100KR2J-1-GP

100KR2J-1-GP

100KR2J-1-GP

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100KR2J-1-GP

49D9R2F-GP

750R2F-GP

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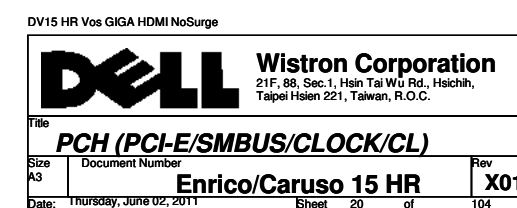
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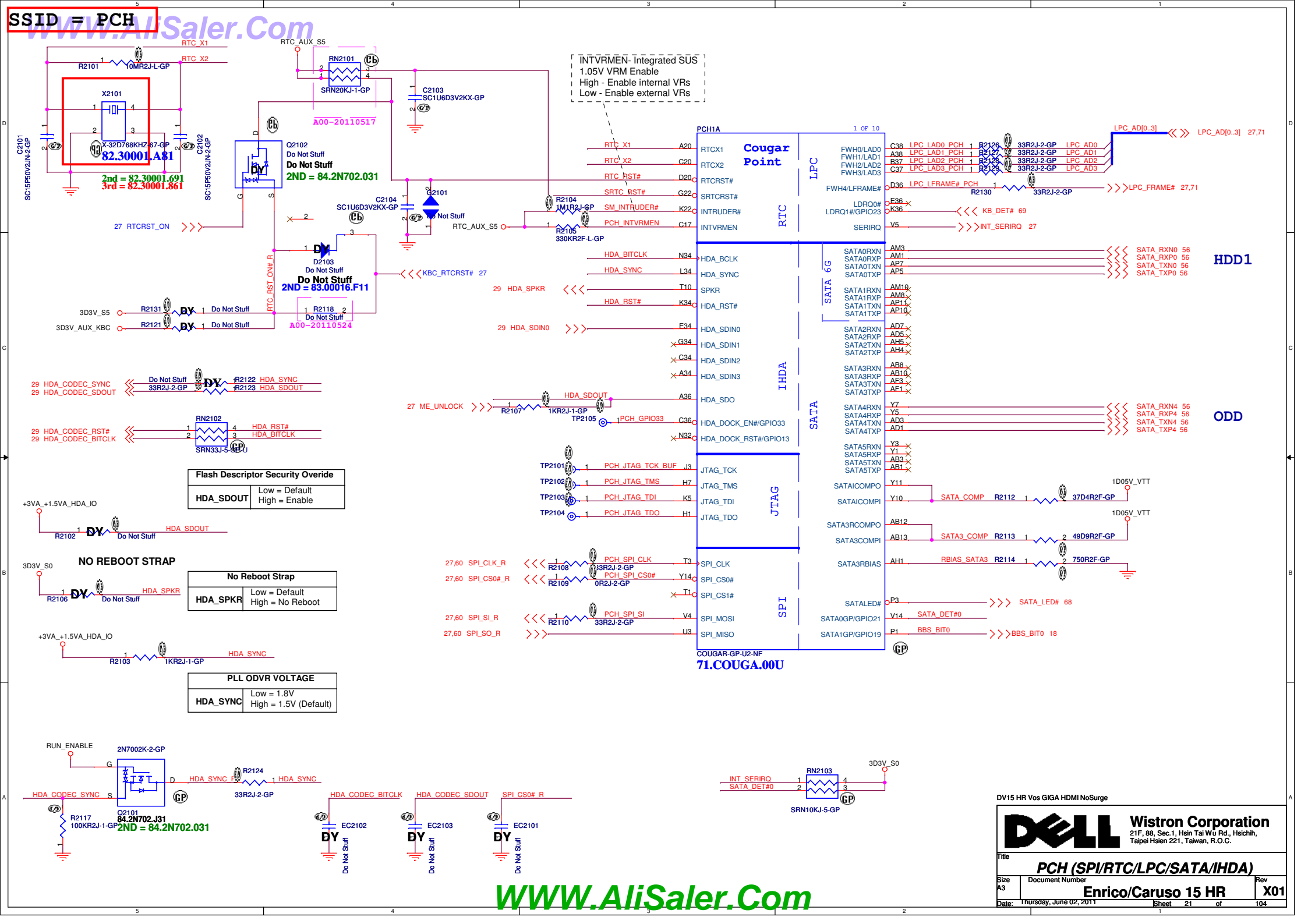
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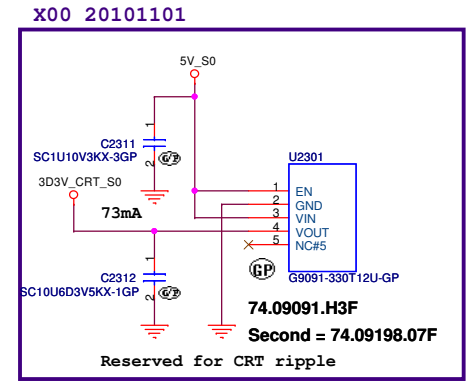
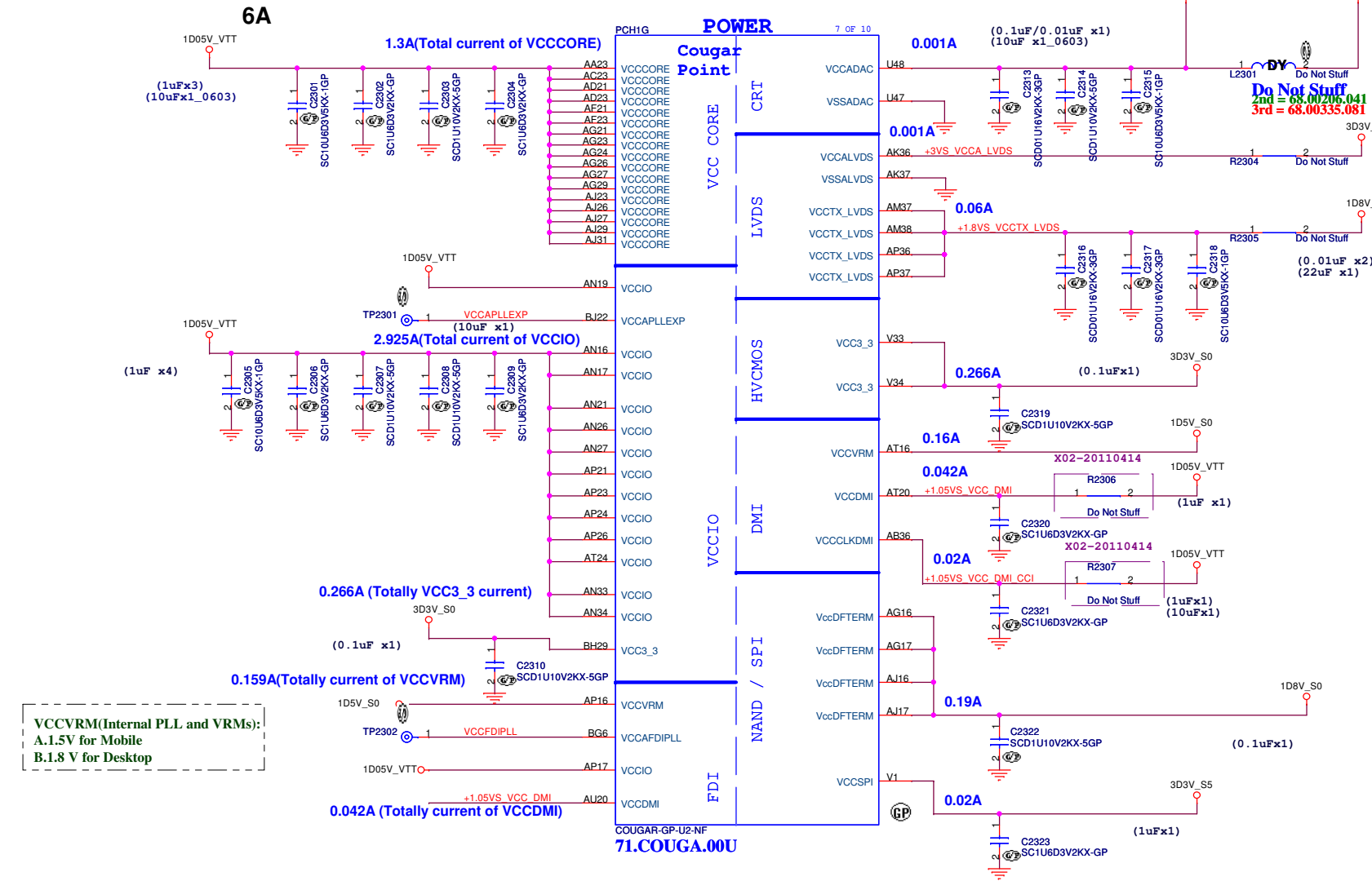


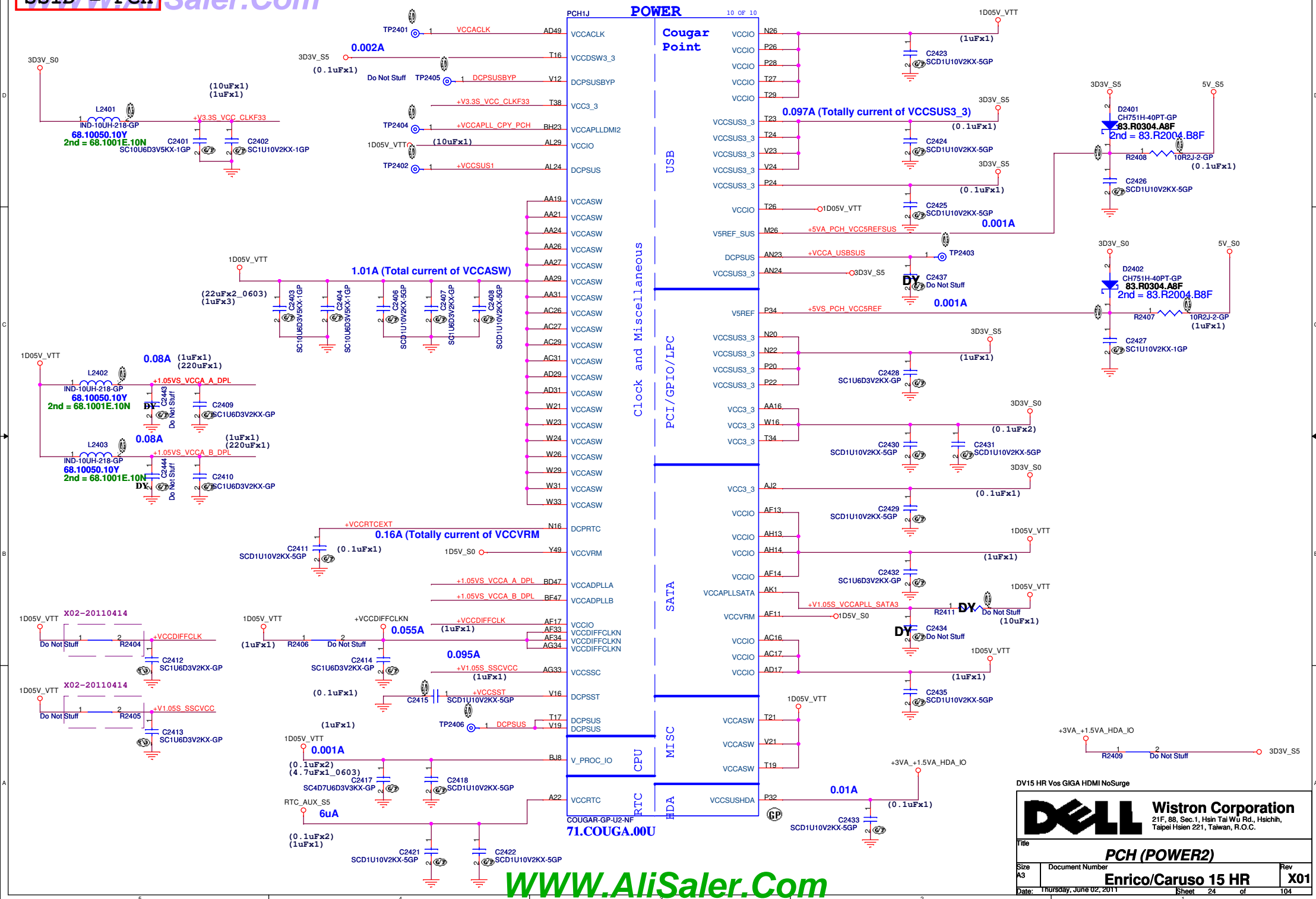


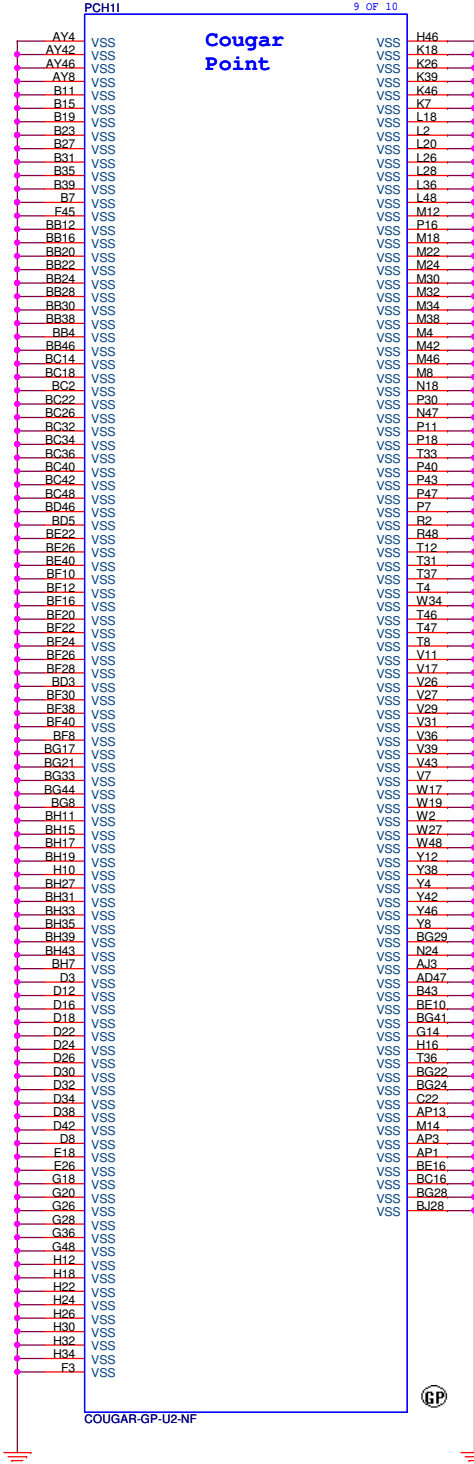
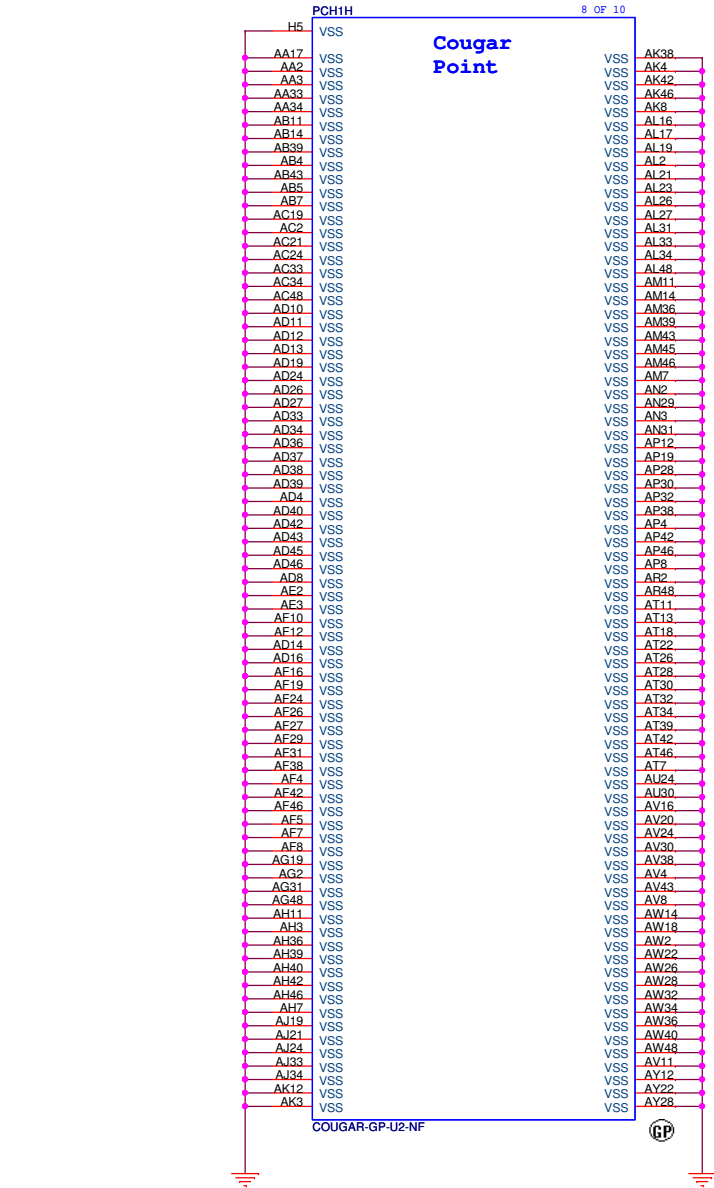




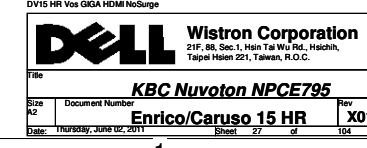






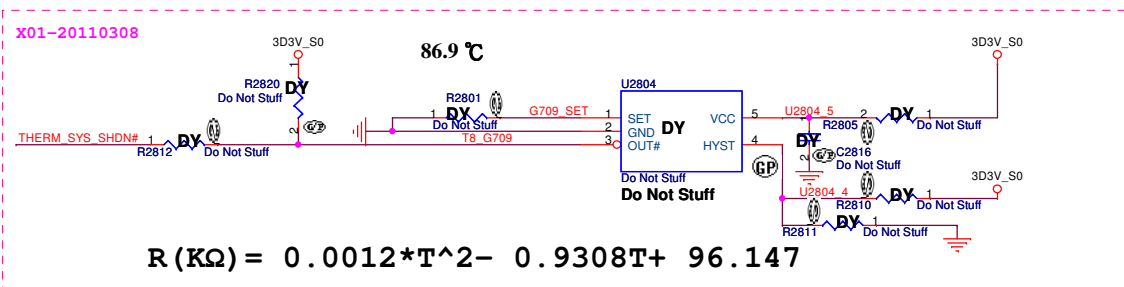
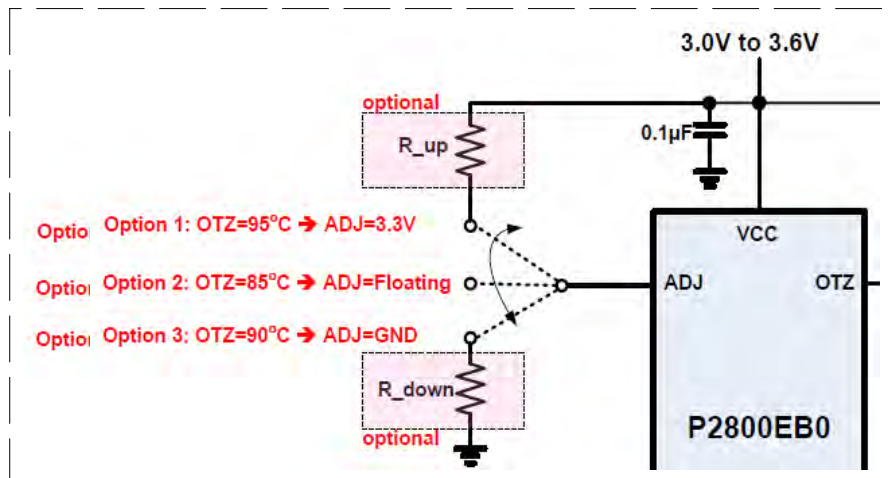
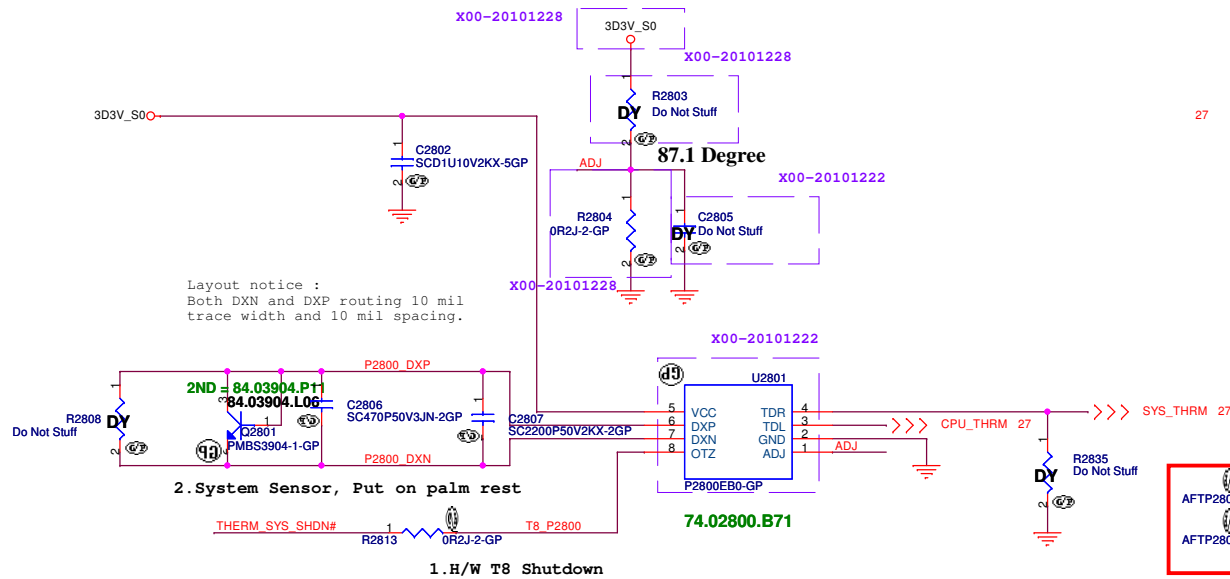


MODEL_ID_DET(GPI07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DV14_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
DV14_DIS_PX	100.0K	20.0K(64.20025.6DL)	2.75V
DV15_UMA with HDMI	100.0K	33.0K	2.48V
DV15_UMA without HDMI	100.0K	47.0K(64.47025.6DL)	2.24V
Reserved	100.0K	64.9K(64.64925.6DL)	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

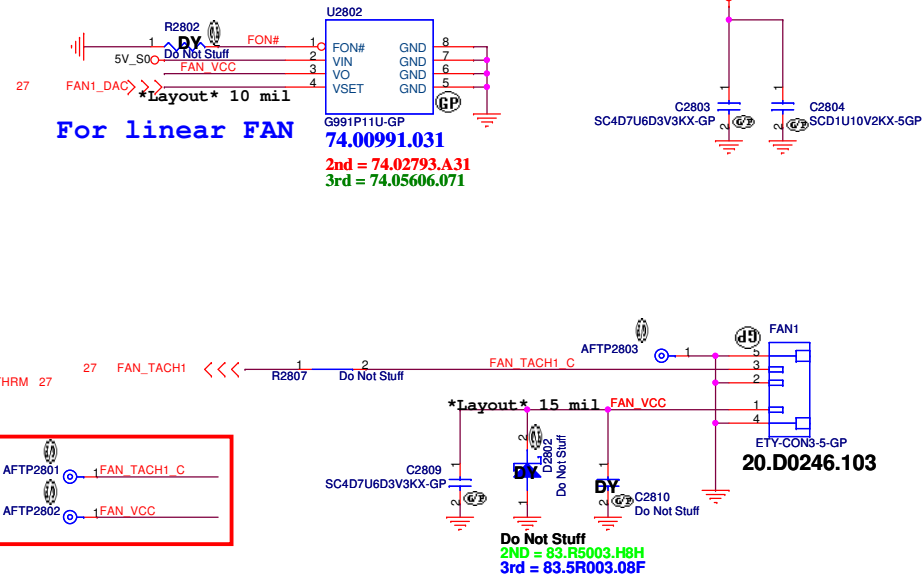
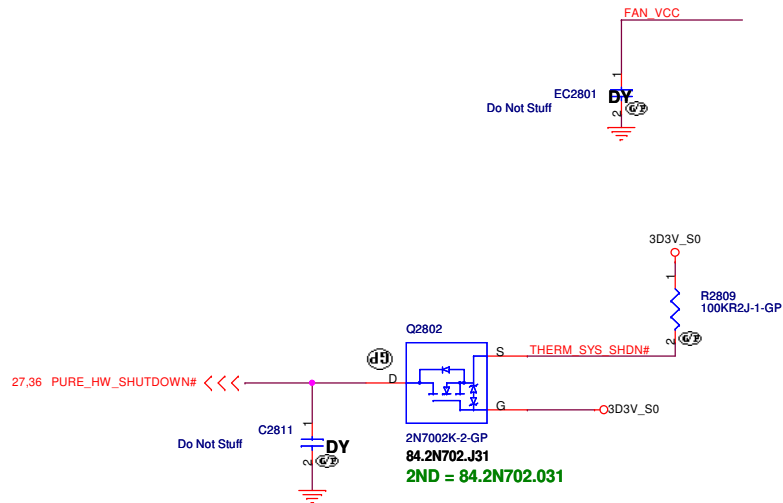




### *Thermal sensor P2800*



## Fan controller G991

**EMI/ESD**

DV15 HR Vos GIGA HDMI NoSurge

DELL

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title  
**Thermal P2800/Fan Controllor P2793**

Size A3	Document Number <b>Enrico/Caruso 15 HR</b>	Rev <b>X01</b>
Date: Thursday, June 02, 2011	Sheet 28 of 104	





# LAN CHIP

60 mils

40 mils

GIGAGIGAGIGA

GIGA

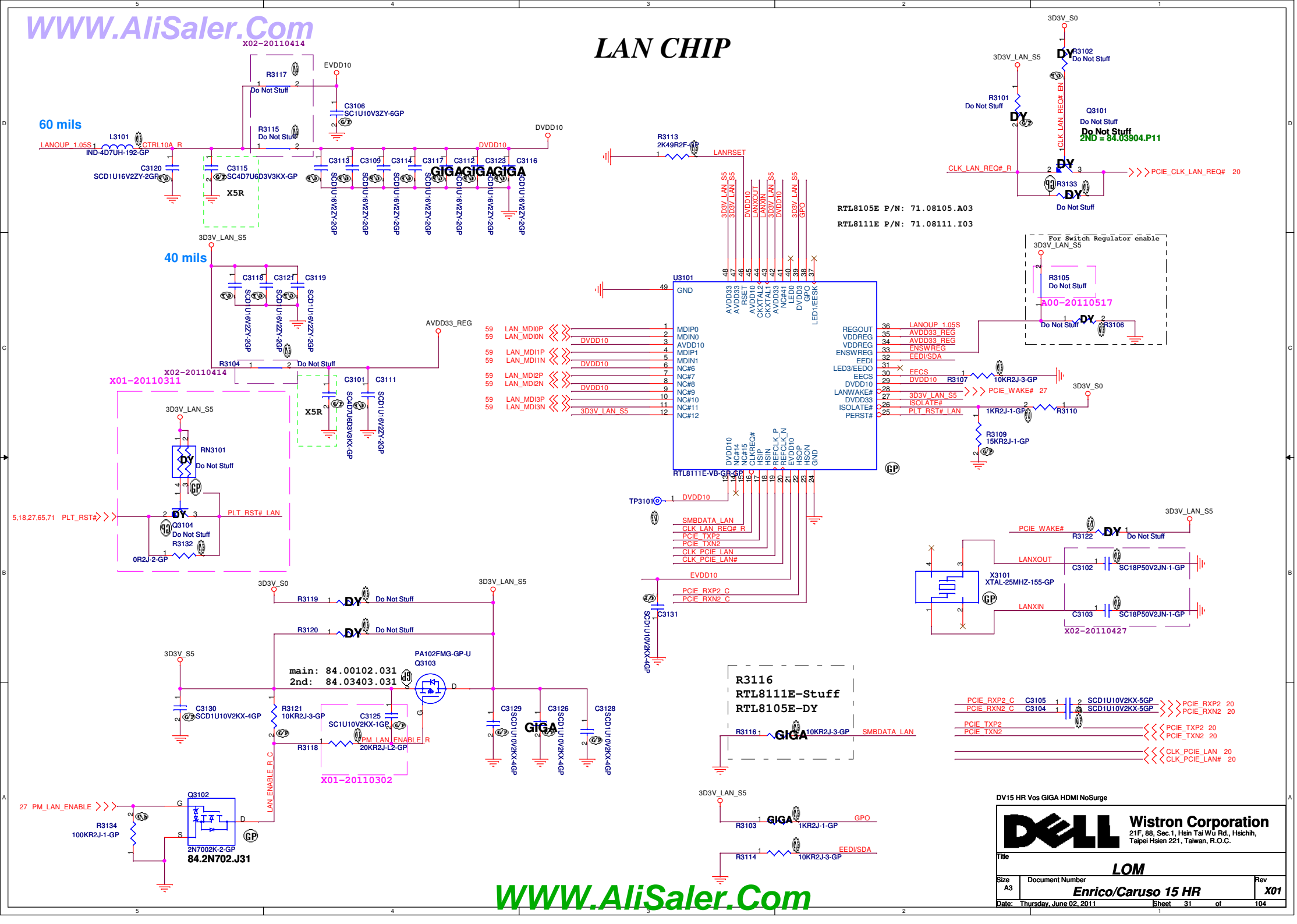
RTL8105E P/N: 71.08105.A03  
RTL8111E P/N: 71.08111.I03

DV15 HR Vos GIGA HDMI NoSurge



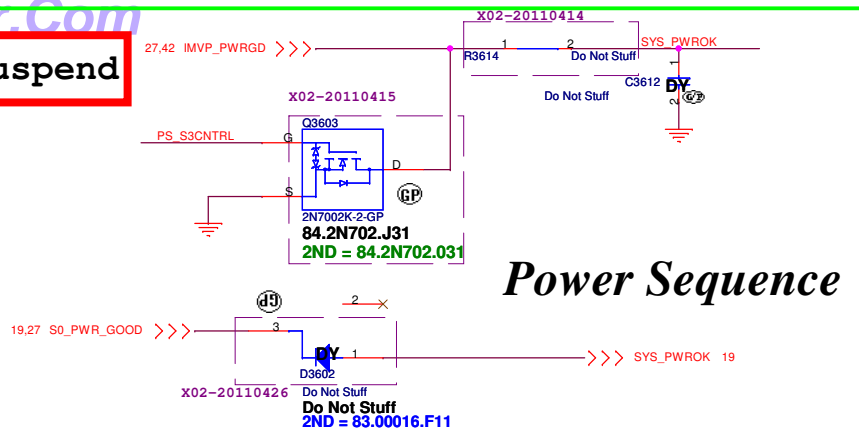
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LOM		
Size A3	Document Number	Rev
	Enrico/Caruso 15 HR	X01
Date: Thursday, June 02, 2011	Sheet 31	of 104

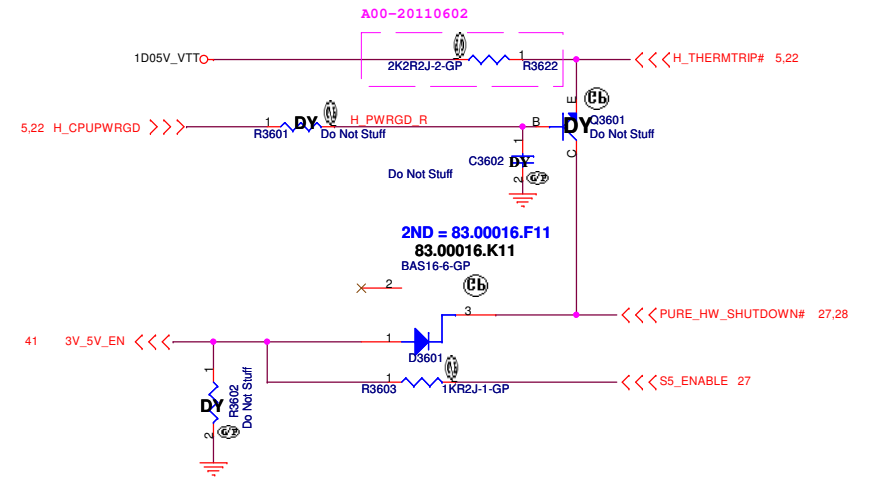
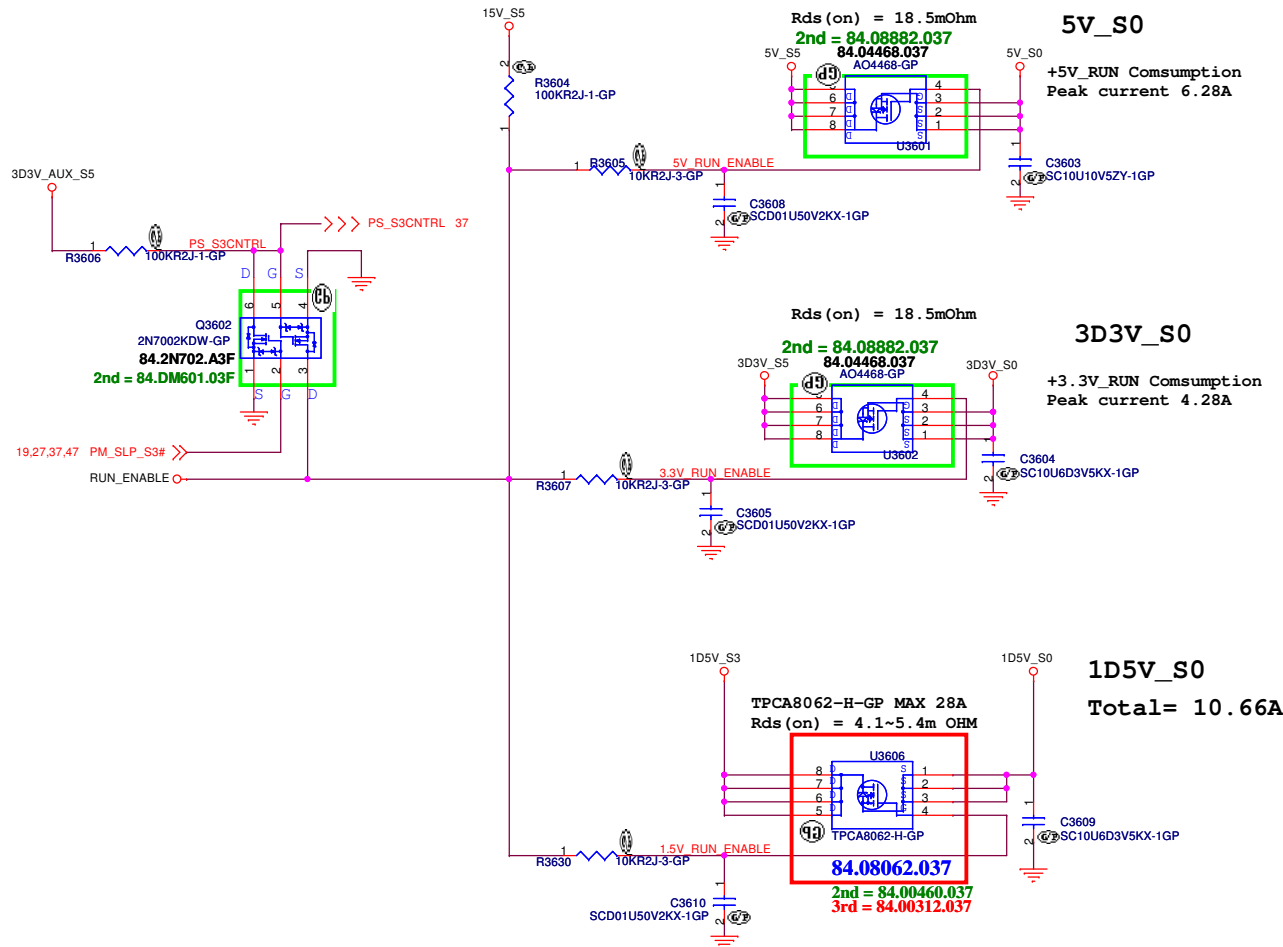




SSID = Reset.Suspend



ROSA Run Power



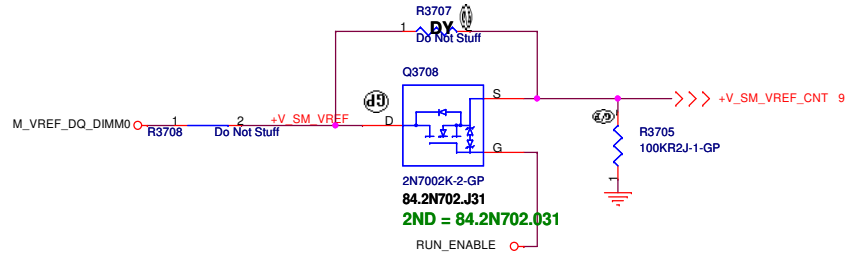
DV15 HR Vos GIGA HDMI NoSurge



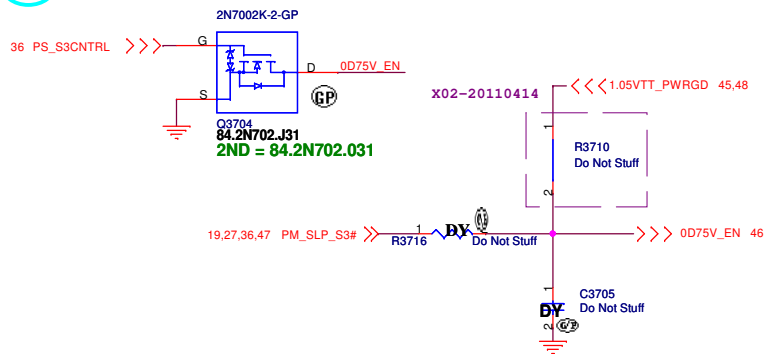
**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
Power Plane Enable			
Size	Document Number		Rev
A3	Enrico/Caruso 15 HR		X01
Date:	Thursday, June 02, 2011	Sheet 36 of	104

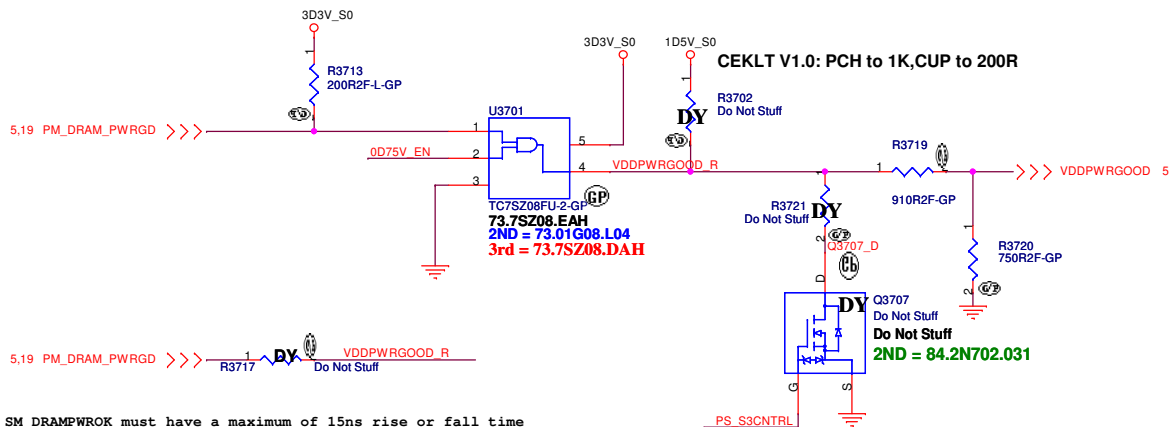
Close to CPU  
S3 Power Reduction Circuit Processor VREF\_DQ Implementation



5 S3 Power Reduction

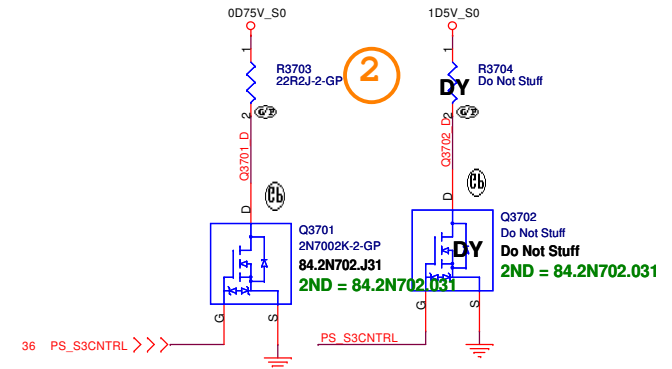


Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK

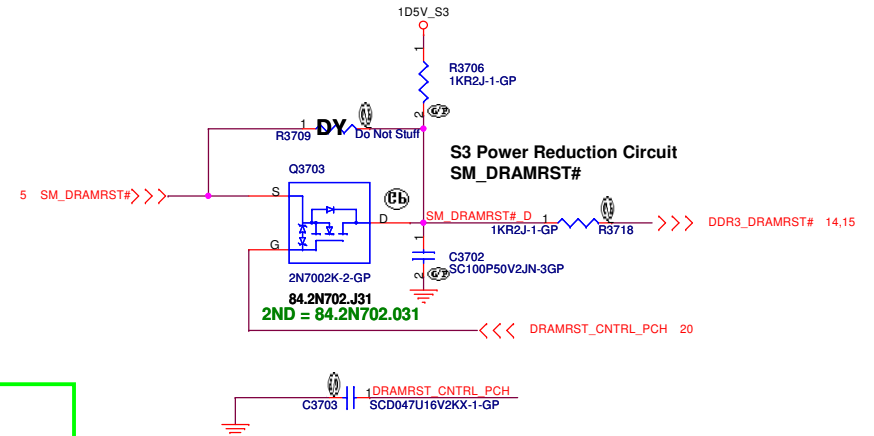


SM\_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ \* 0.55± 200mV and the edge must be monotonic

Close to DIMM  
S3 Power Reduction Circuit SM\_DRAMPWROK

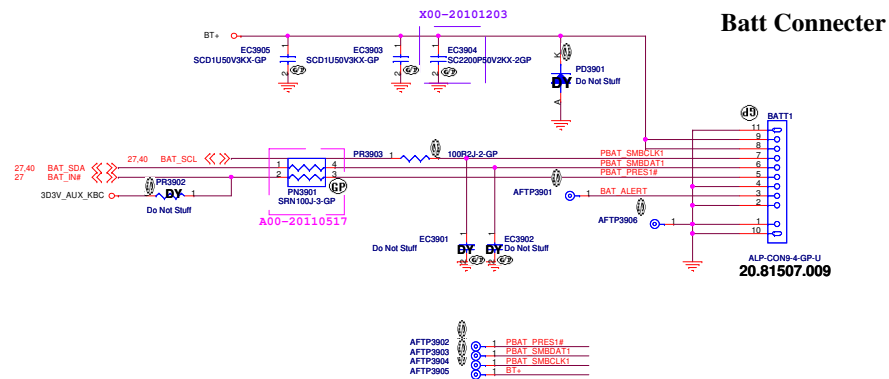


Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK

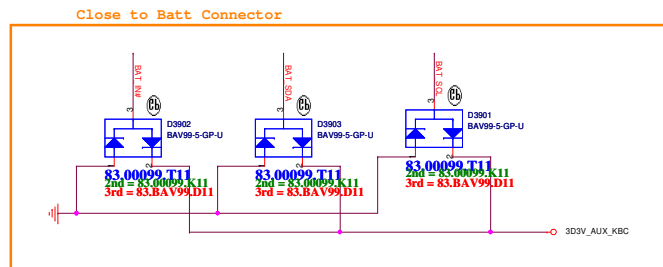


DV15 HR Vos GIGA HDMI NoSurge





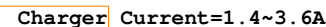
For actual location, need to be swap all pin



DV15 HR Vos GIGA HDMI NoSurge

0802 Rename H\_PROCHOT#

5,27,42 H\_PROCHOT# &lt;&lt;—



EE need check pull high

ROSA

Adapter type	PR4023
65W	24K
90W	33.2K
130W	59K

EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

DV15 HR Vos GIGA HDMI NoSurge



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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466
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**CHARGER BQ24707**

Size	
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Custom **En**

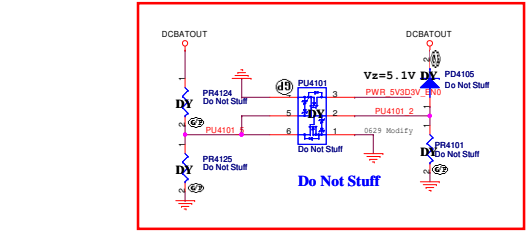
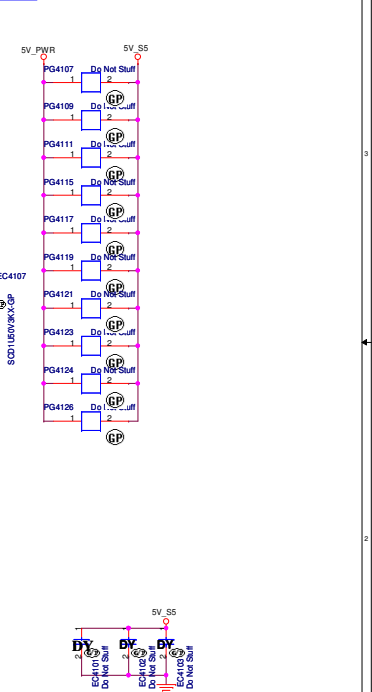
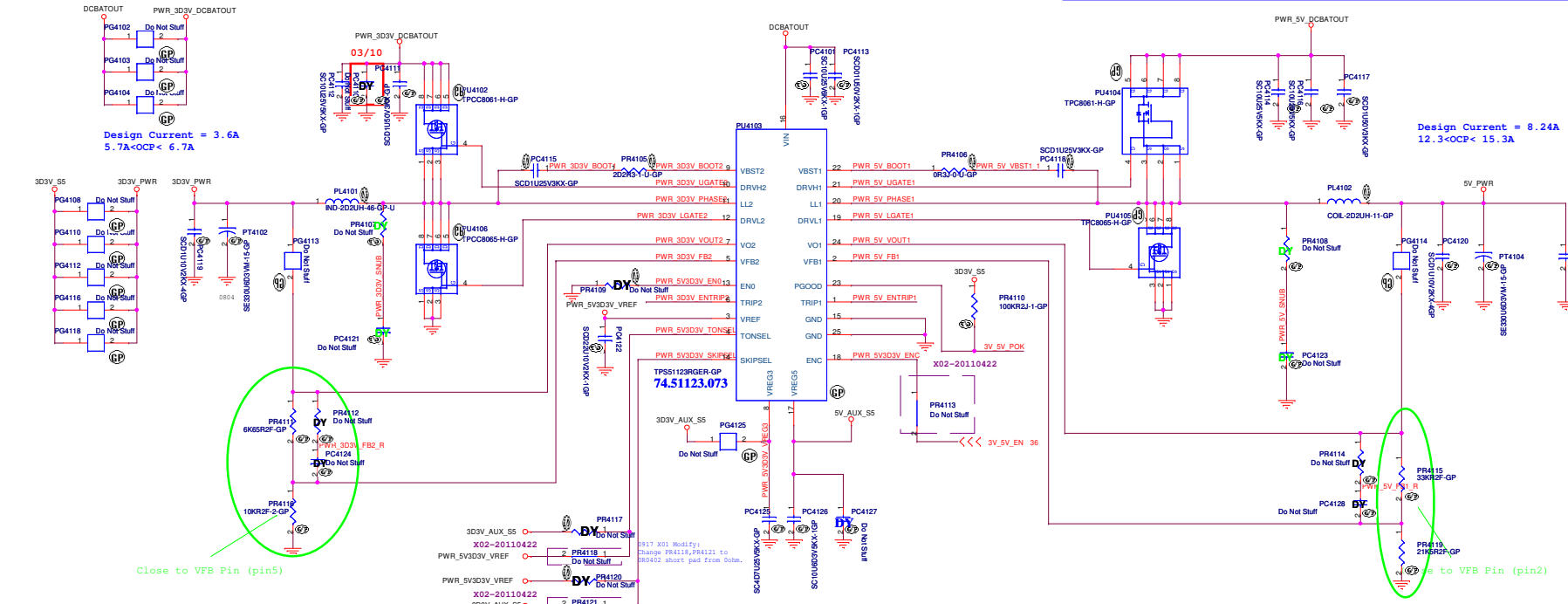
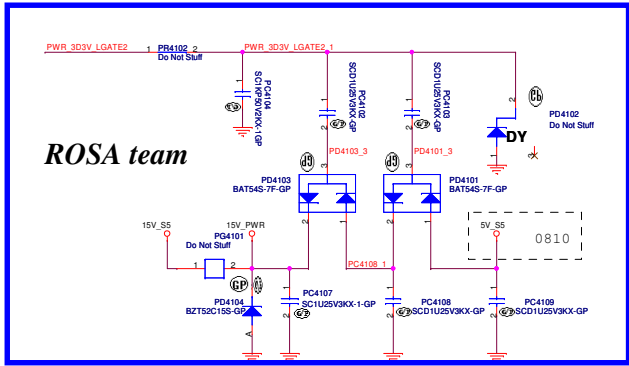
### Enrico/Caruso 15 HR

Date: Thursday, June 02, 2010

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Y01

104



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG5 or VREG5	400kHz	500kHz

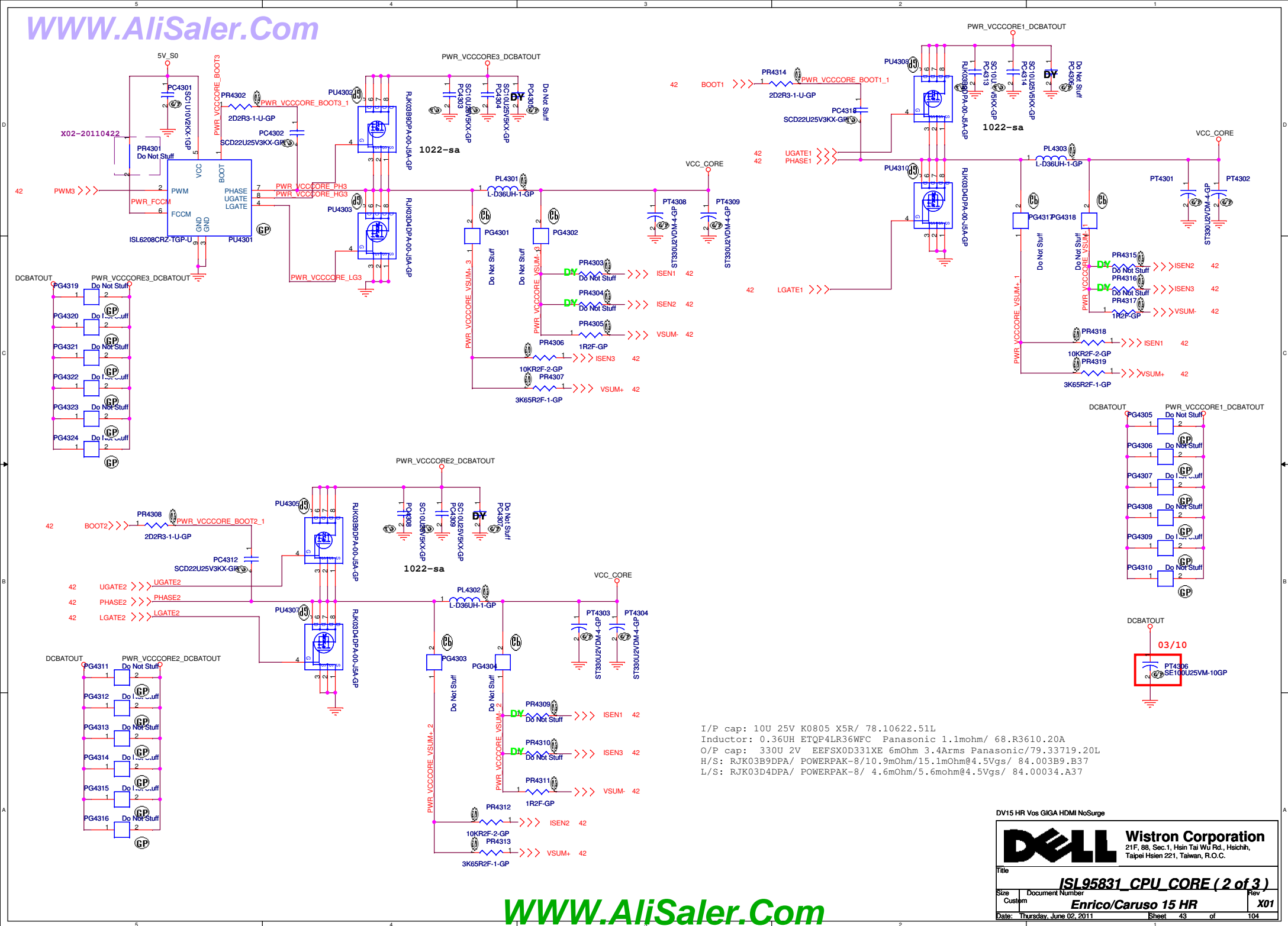
SKIPSEL	VREG5 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: 2.20UH PCMC104T-2R2 Cyntec 7mohm Isat =27Arms 68.2R210.20C  
O/P cap: 330U6.3V M6.3\*5.7 15mOhm 3.16Arms Matsuki/77.53371.04L  
H/S: TPC8061-H / 21mohm/30mOhm@4.5Vgs/ 84.08061.037  
L/S: TPC8065-H / 12mohm/15mOhm@4.5Vgs/ 84.08065.037

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: 2.2U PCMC063T-2R2M Cyntec 20mohm Isat =14Arms 68.2R210.20B  
O/P cap: 330U6.3V M6.3\*5.7 15mOhm 3.16Arms Matsuki/77.53371.04L  
H/S: TPC8061-H NC 8P / 21mohm/29mOhm@4.5Vgs/ 84.08061.A37  
L/S: TPC8065-H NC 8P / 12.1mohm/17.4mOhm@4.5Vgs/ 84.08065.A37







I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
 Inductor: 0.36UH ETQP4LR36WFC Panasonic 1.1mohm/ 68.R3610.20A  
 O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L  
 H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37  
 L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 HR Vos GIGA HDMI NoSurge

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <b>ISL95831 CPU CORE (2 of 3)</b>	
Size	Document Number	Rev <b>Enrico/Caruso 15 HR</b>	
Date: Thursday, June 02, 2011	Sheet 43	of 104 X01	



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**ISL95831\_CPU\_CORE(3/3)**

Size

Document Number

## Enrico/Caruso 15 HR

Rev

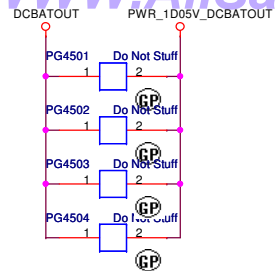
Date: Thursday, June 02, 201

Sheet 4

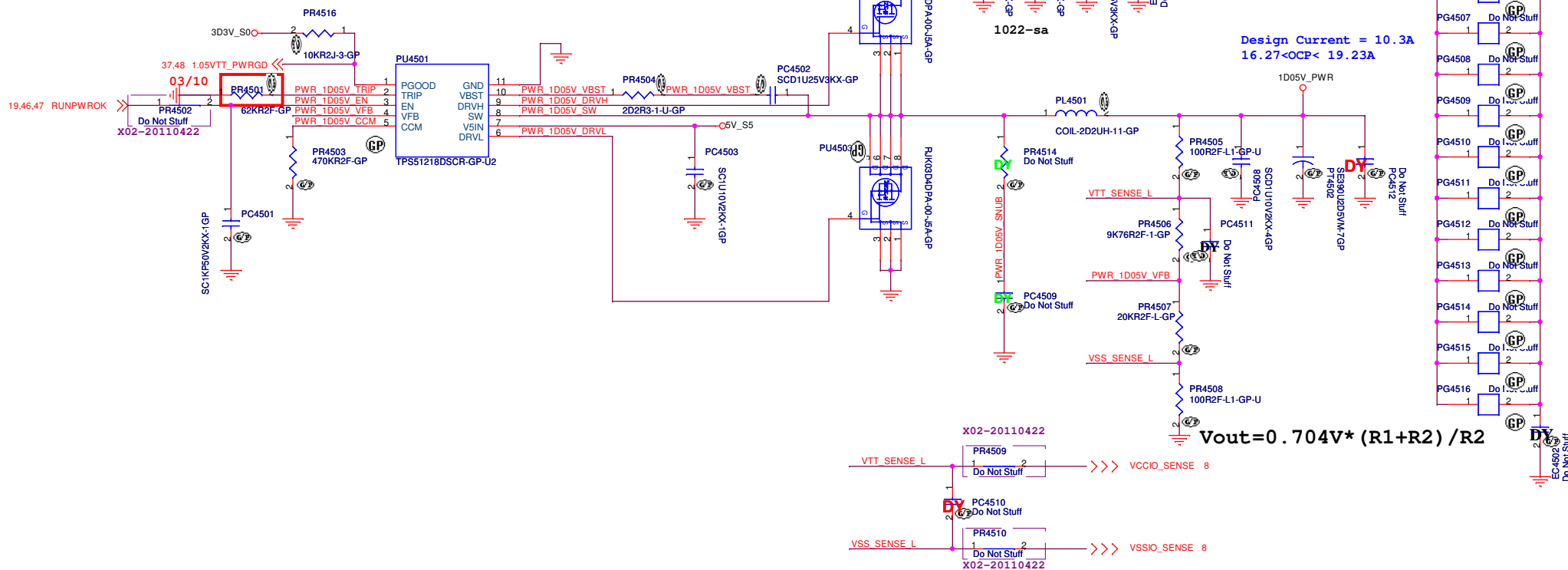
44

of

104



## TPS51218 for 1D05V



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: 2.20UH PCMC104T-2R2 Cyntec 7mohm Isat =27Arms 68.2R210.20C  
O/P cap: 390U 2.5V M 6.3\*5.7/ 10mOhm 3.87Arms Matsuki/ 79.3971V.30L  
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37  
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 HR Vos GIGA HDMI NoSurge



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title
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**TPS51218\_+1.05V\_VTT**Size  
A3

Document Number
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## Enrico/Caruso 15 HR

Date \_\_\_\_\_

Thursday, June 02, 2010

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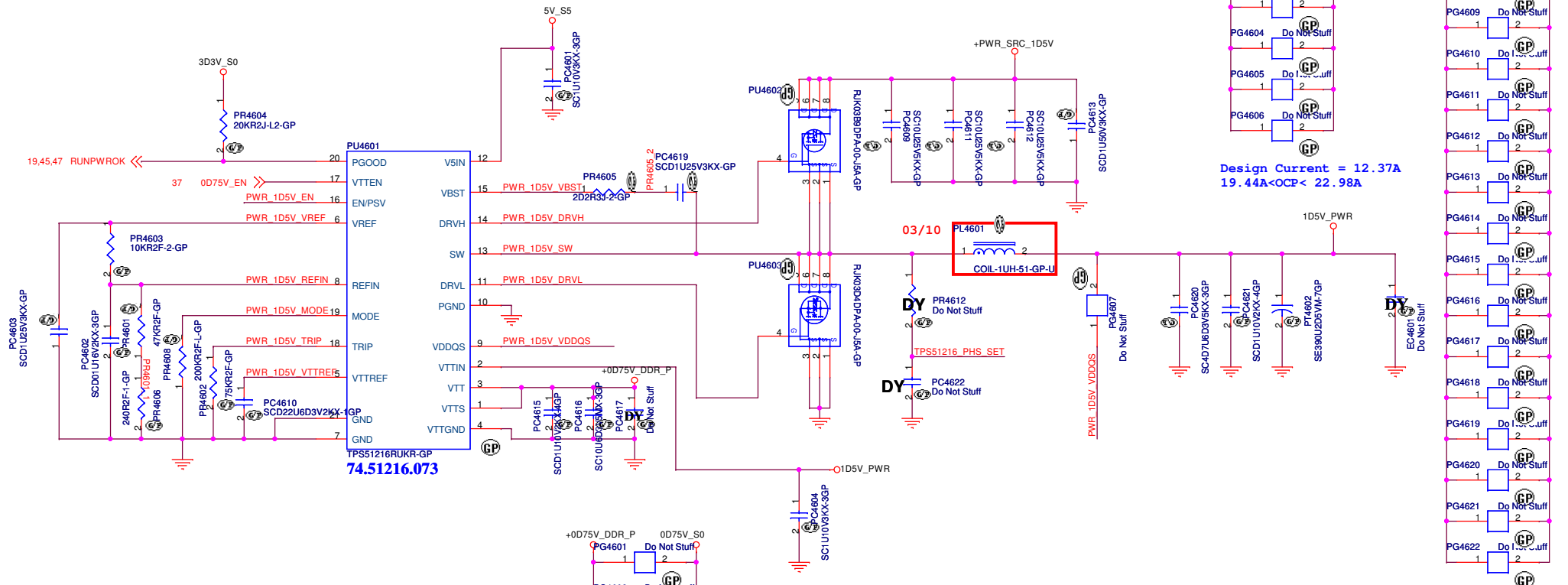
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Rev	
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**X01**

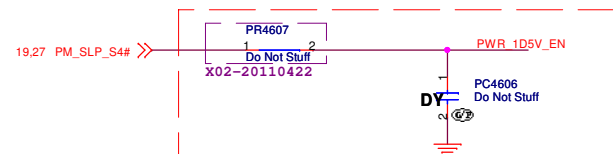
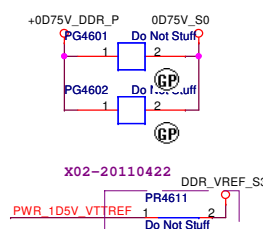
104

SSID = PWR.Plane.Regulator 1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	Frequency	Discharge Mode
PR4608	400kHz	Tracking Discharge
200k ohm	300kHz	
100k ohm	300kHz	Non-tracking Discharge
68k ohm	300kHz	
47k ohm	400kHz	



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
 Inductor: 1.0UH PCMB104T-1R0M Cyntec 3mohm Isat =28Arms 68.1R01C.10Q  
 O/P cap: 390U 2.5V M 6.3\*5.7/ 10mOhm 3.87Arms Matsuki/79.3971V.30L  
 H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37  
 L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

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File

**TPS51116 +1.5V SUS**

Size A3 Document Number

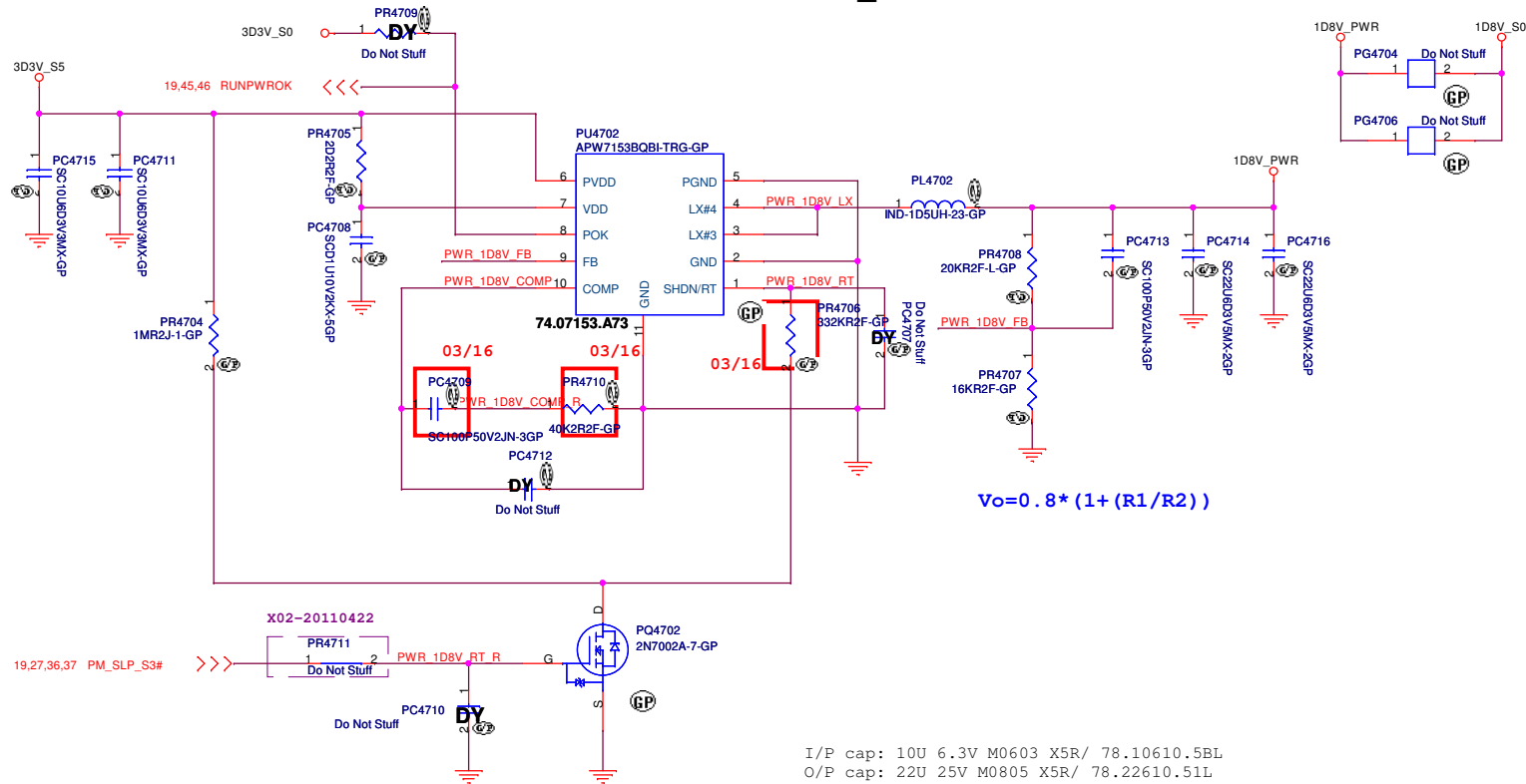
**Enrico/Caruso 15 HR**

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Rev **X01**

## APW7153B for 1D8V\_S0

+1.8V\_RUN  
Design current = 0.87A



I/P cap: 10U 6.3V M0603 X5R/ 78.10610.5BL  
O/P cap: 22U 25V M0805 X5R/ 78.22610.51L  
Inductor: 1.5U PCMC063T Cyntec 14mohm/15mohm Isat =18Arms 68.1R510.10K

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DELL

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Title
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**TPS51311 for 1D8V\_S0**Size  
A2

Document Number
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### Enrico/Caruso 15 HR

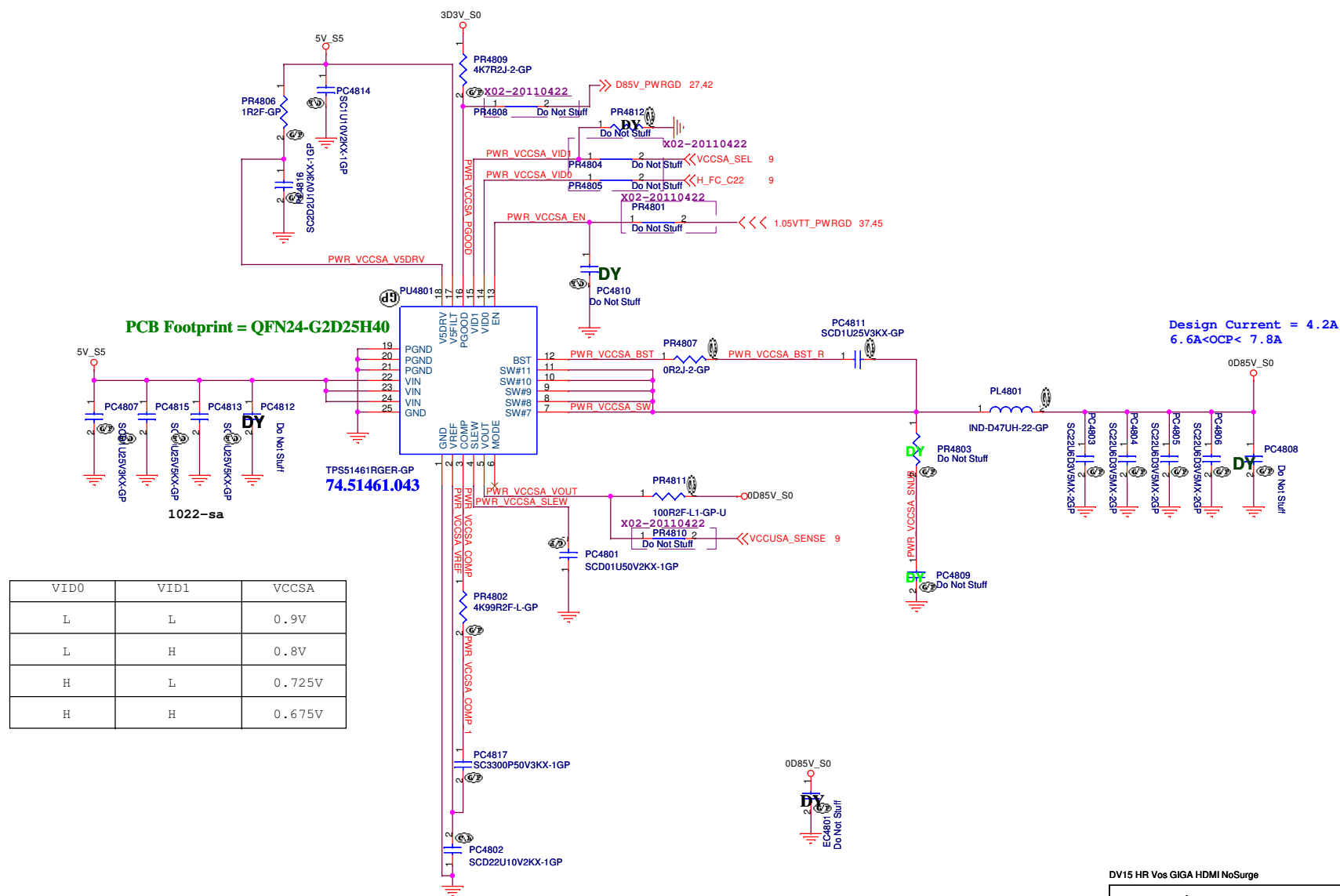
Rev
<b>X01</b>

Date: Thursday, June 02, 2011

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# TPS51461 for VCCSA



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Title			<b>TPS51461 VCCSA</b>	
Size	Document Number	Rev		
A3		<b>Enrico/Caruso 15 HR</b>		<b>X01</b>
Date:	Thursday, June 02, 2011	Sheet	48	of 104



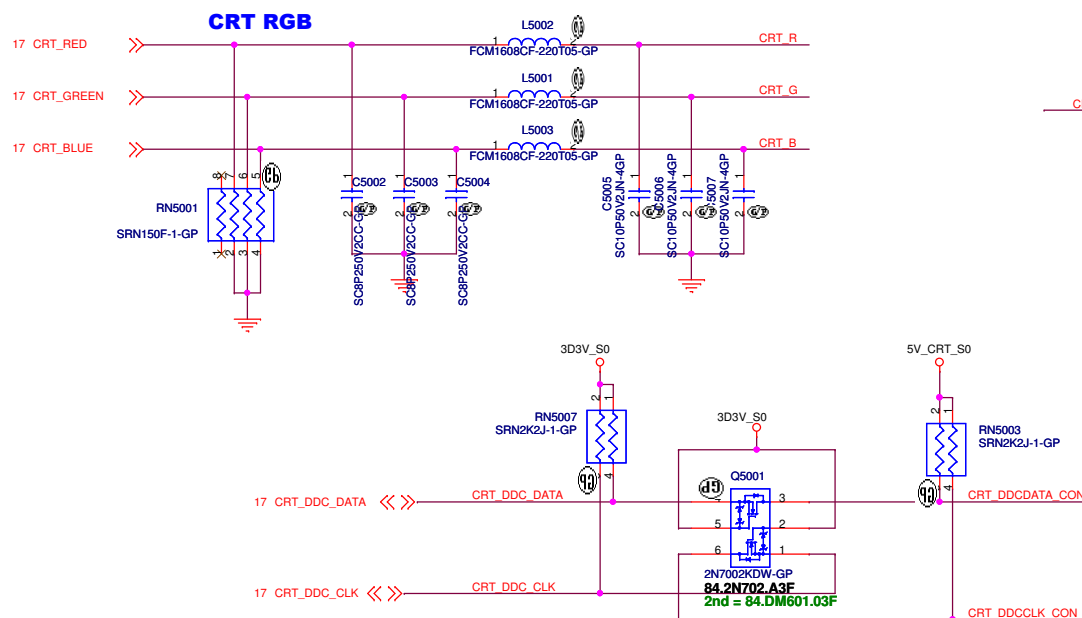


SSID = VIDEO

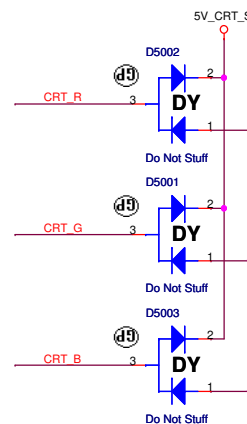
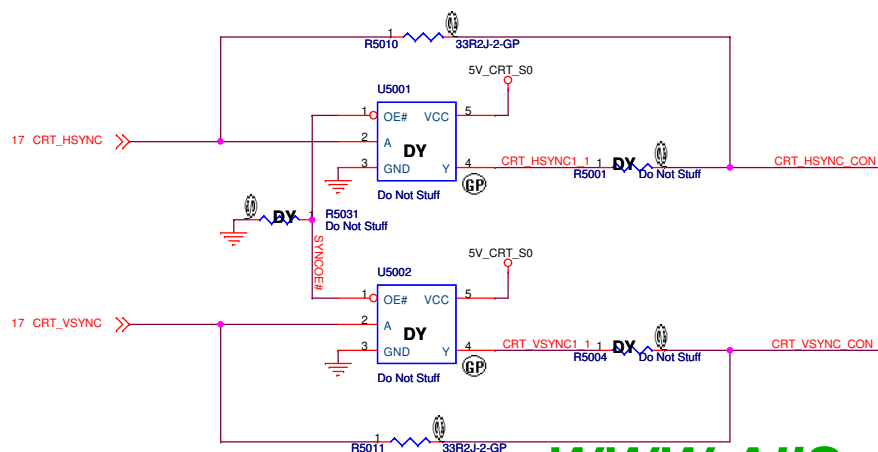
Layout Note:

\*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.

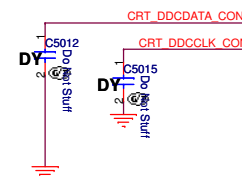
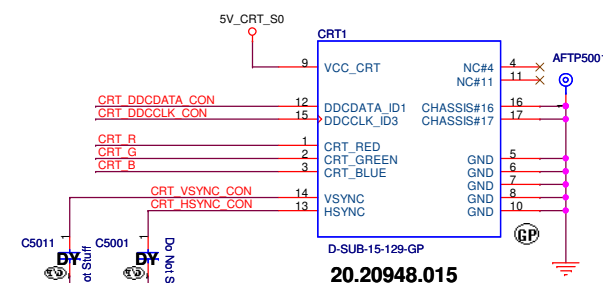
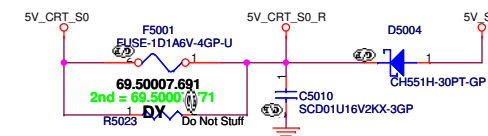
\* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



### Hsync & Vsync

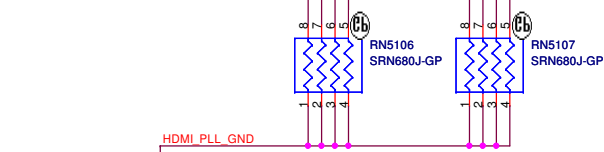
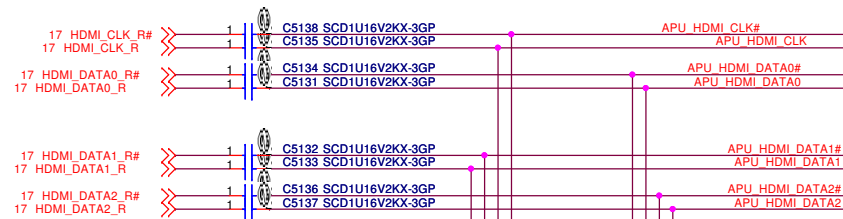


AFTP5002 1 5V CRT\_S0  
AFTP5003 1 CRT\_DDCDATA\_CON  
AFTP5004 1 CRT\_DDCCLK\_CON  
AFTP5005 1 CRT\_R  
AFTP5006 1 CRT\_G  
AFTP5007 1 CRT\_B  
AFTP5008 1 CRT\_HSYNC\_CON  
AFTP5009 1 CRT\_VSYNC\_CON



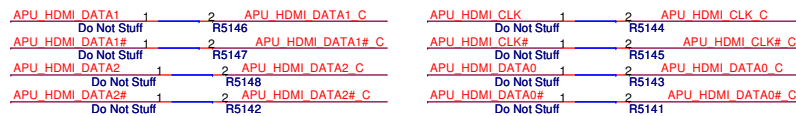
DV15 HR Vos GIGA HDMI NoSurge

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>CRT Connector</b>			
Size Custom	Document Number	<b>Enrico/Caruso 15 HR</b>	Rev <b>X0</b>
Date: Thursday, June 02, 2011	Sheet 50 of 104		104

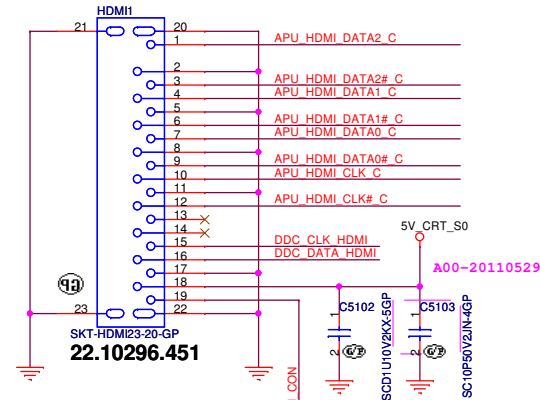


17 PCH\_HDMI\_CLK >>>

17 PCH\_HDMI\_DATA <<<



## HDMI CONN



5V\_CRT\_S0

3D3V\_S0

Do Not Stuff

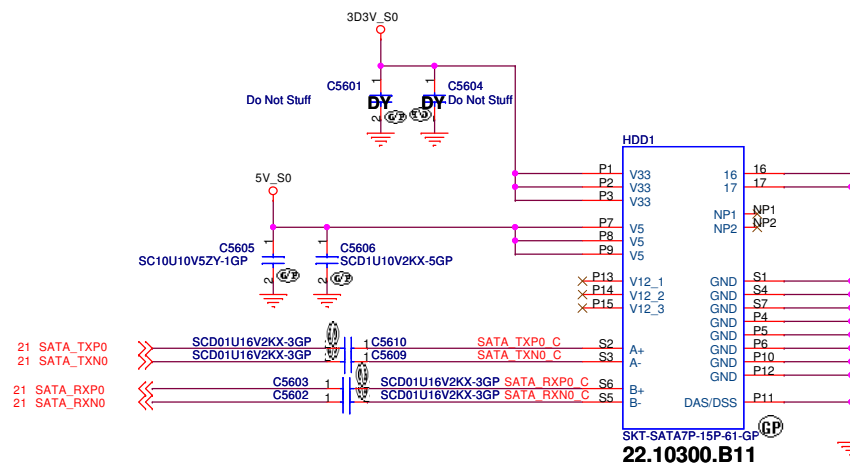
84.03904.L06  
2nd = 84.03904.P11  
3rd = 84.03904.T11

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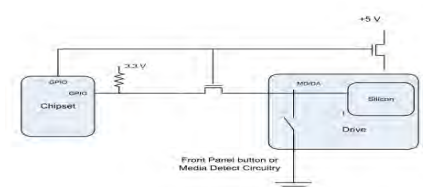
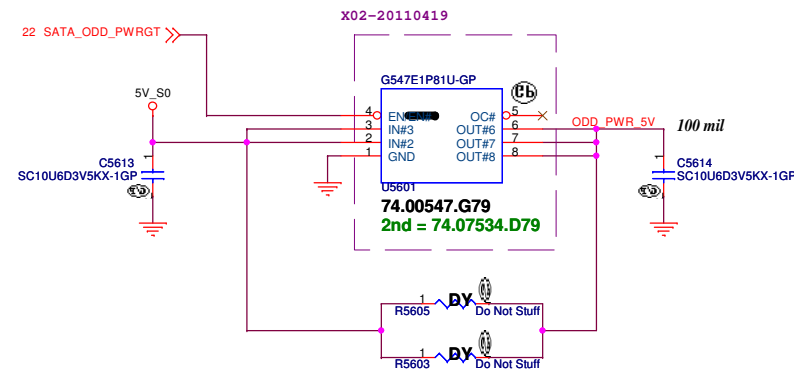
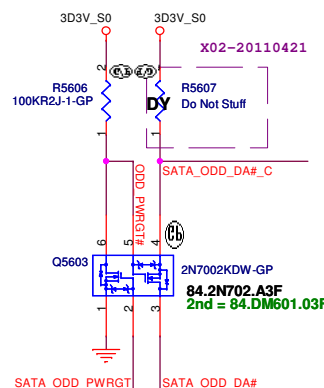
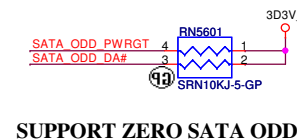
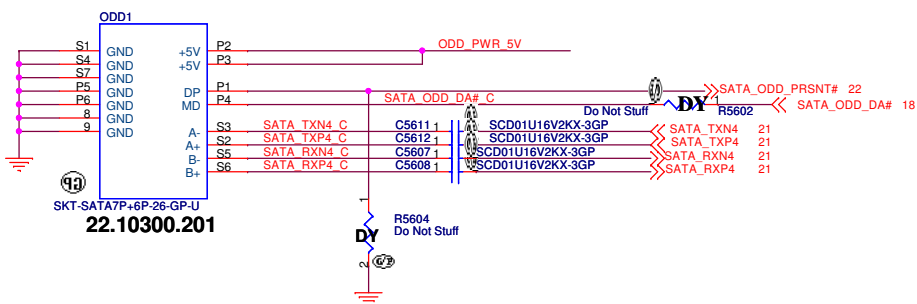
<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: <b>HDMI Level Shifter/Connector</b>			
Size: A3	Document Number: <b>Enrico/Caruso 15 HR</b>	Rev: <b>X01</b>	
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SSID = SATA

## SATA HDD Connector



## ODD Connector



When the drive is powered on, the FET to the MD/DA pin drive is OFF.  
When the drive is powered off, the FET to the MD/DA pin is ON

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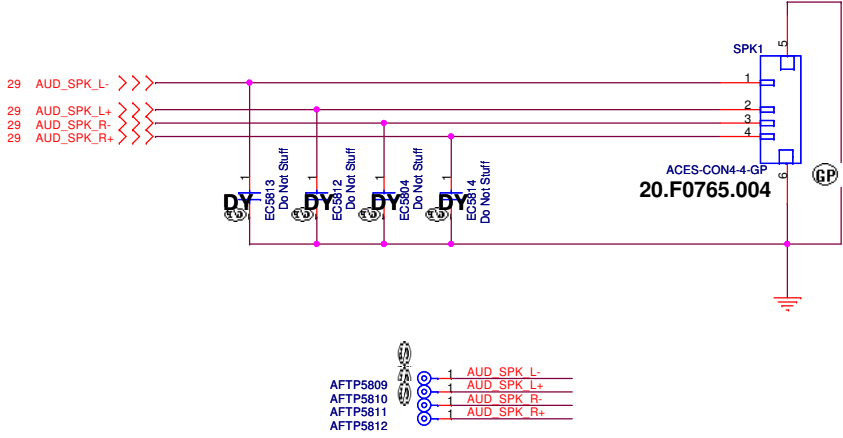


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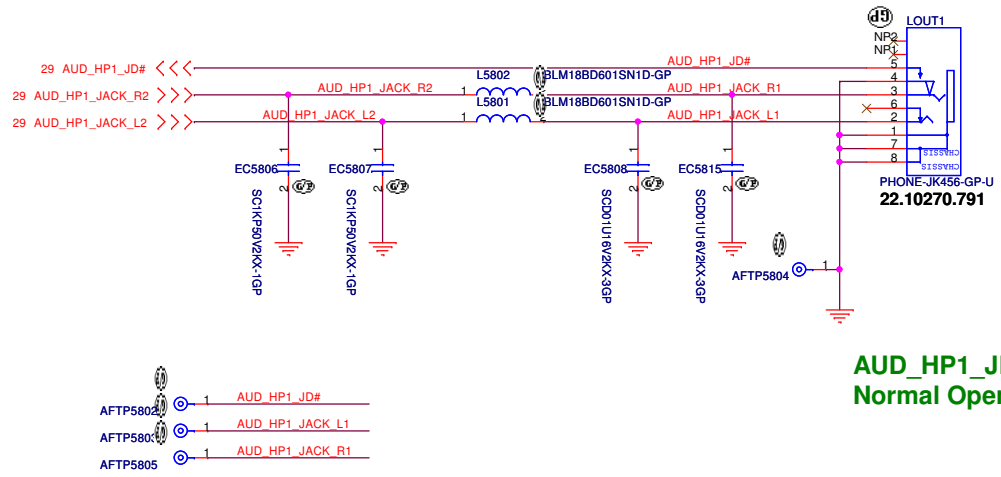
Title			
HDD/ODD			
Size	Document Number	Rev	
A3			
Enrico/Caruso 15 HR			X01
Date:	Thursday, June 02, 2011	Sheet	56 of 104

SSID = AUDIO

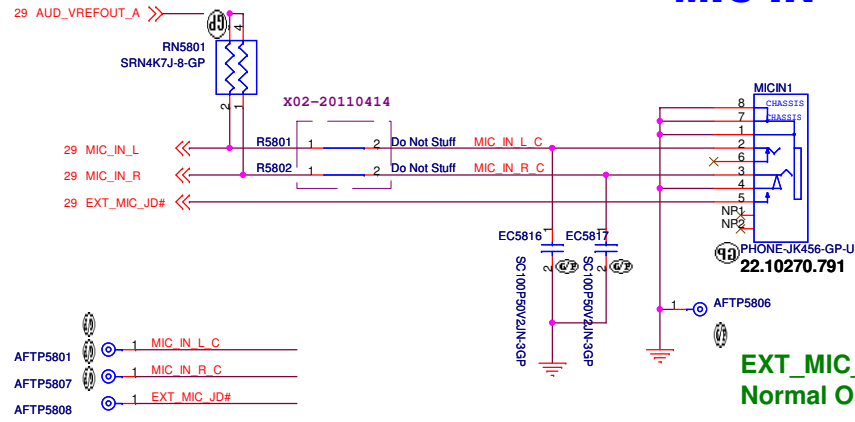
## Speaker Connector



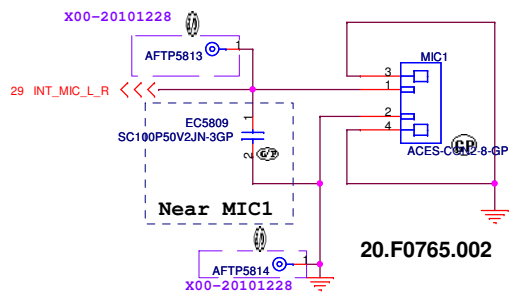
## LINE1 OUT



## MIC IN



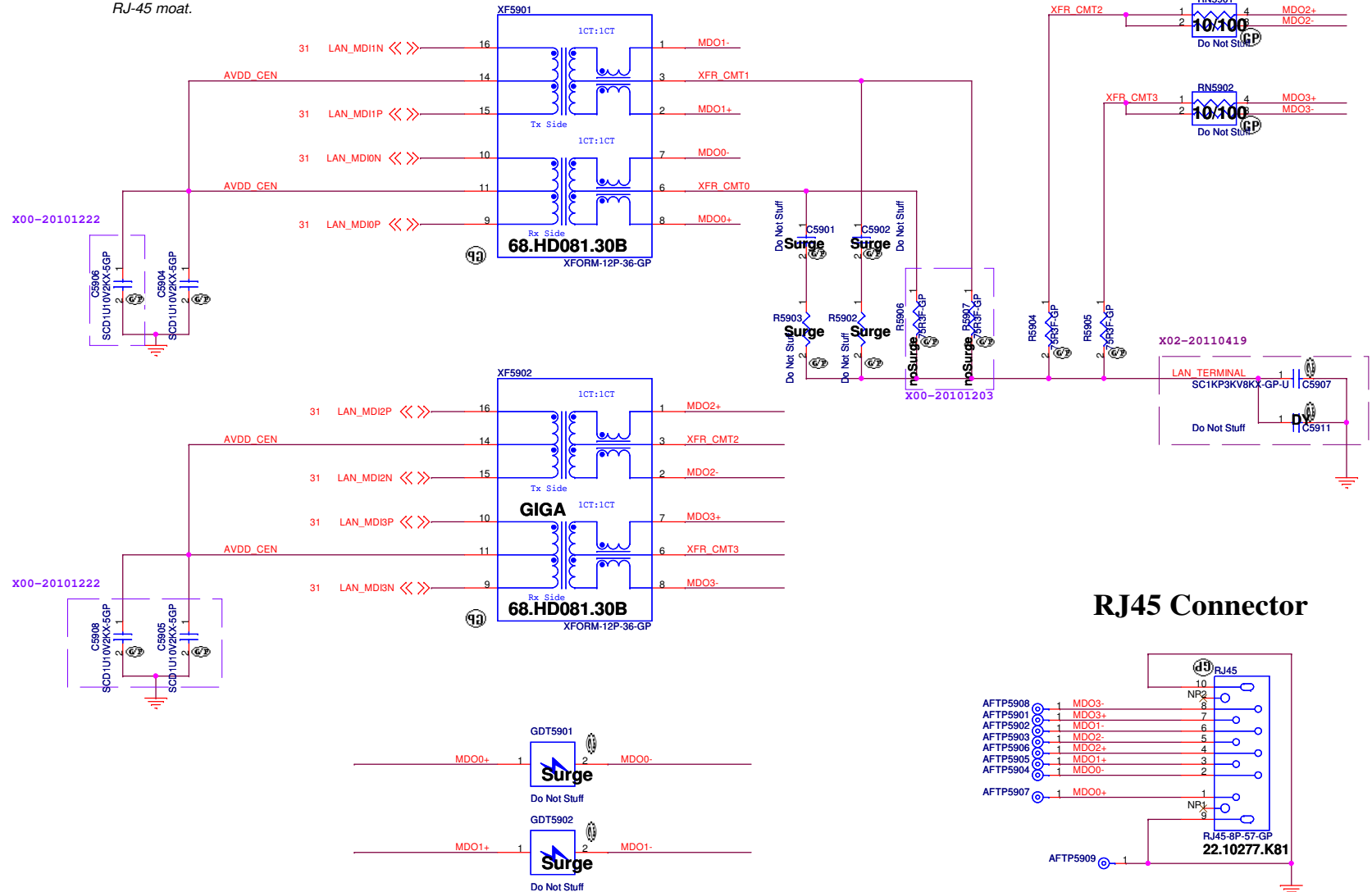
## Internal Microphone



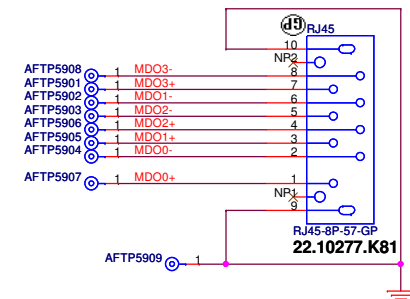
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- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

### 10/100M Lan Transformer



### RJ45 Connector



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Title

## Flash/RTC

Size  
A3

Document Number	
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## Enrico/Caruso 15 HR

Rev	X01
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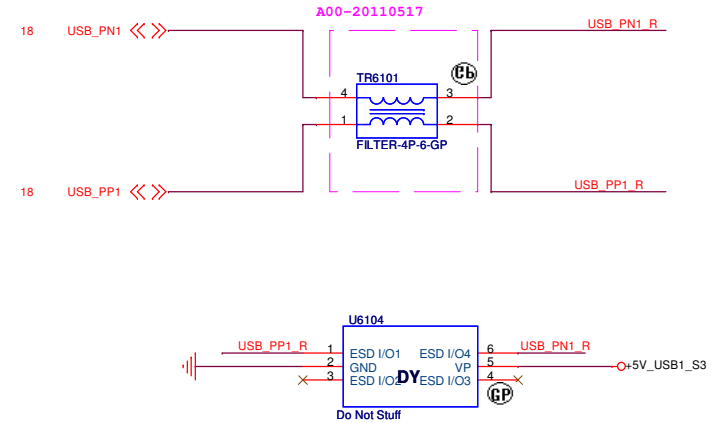
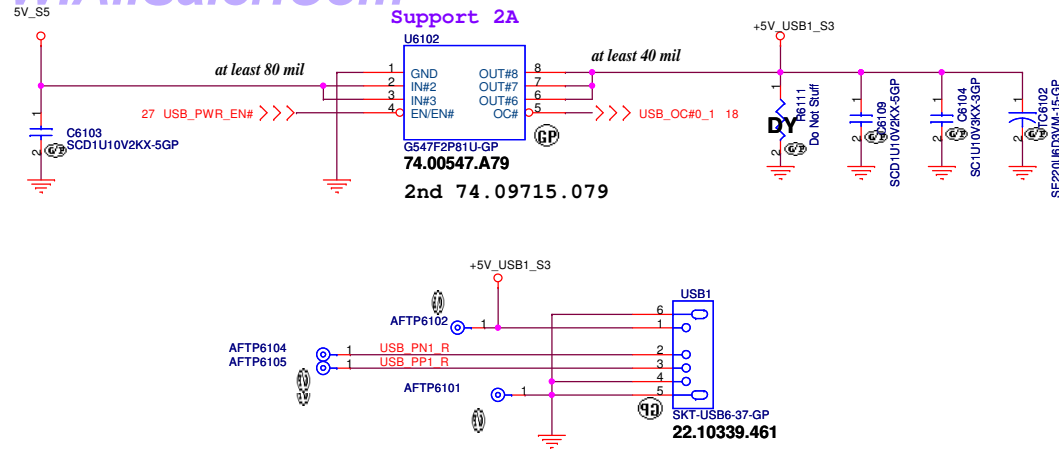
Date: Thursday, June 02, 2011

Sheet 6

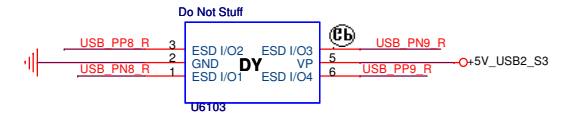
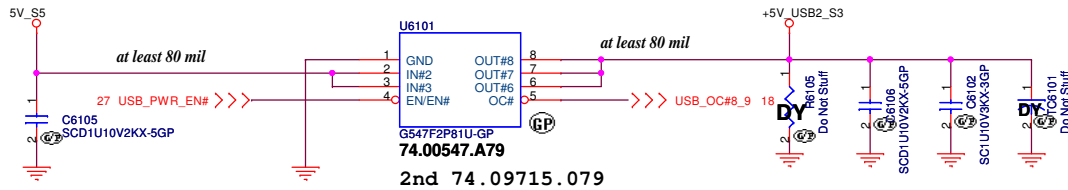
104

SSID = USB

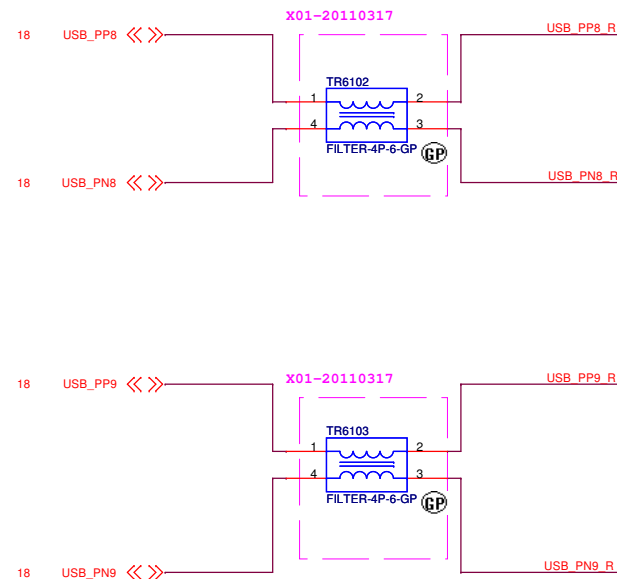
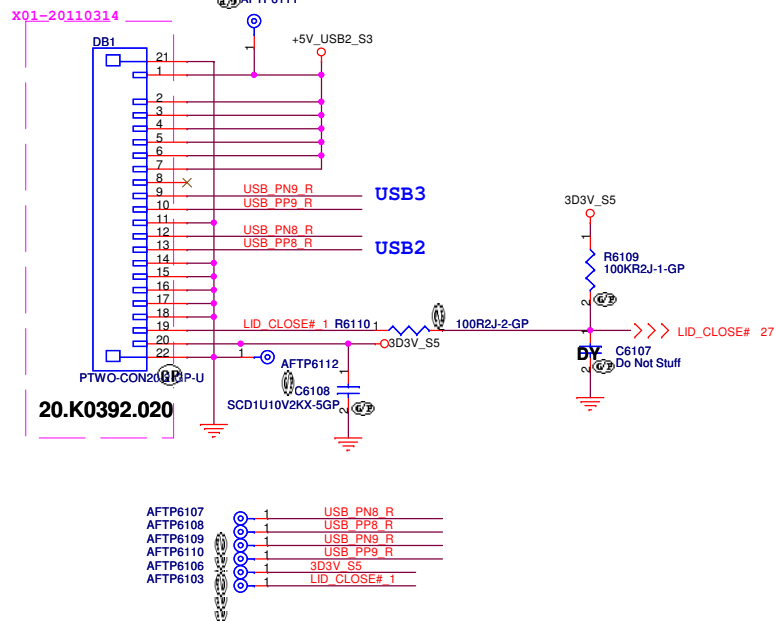
## Left USB Power x1



## Right USB Power x2



Pitch=0.5mm



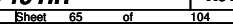
DV15 HR Vos GIGA HDMI NoSurge



USB Power SW			Rev
Size	Document Number	X01	
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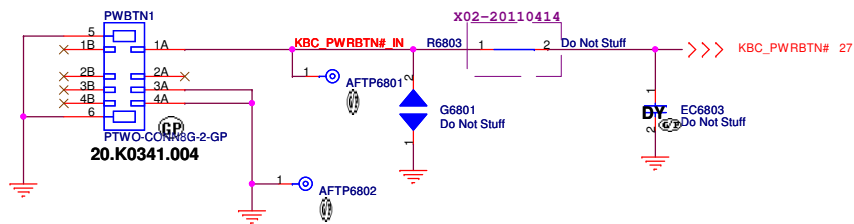


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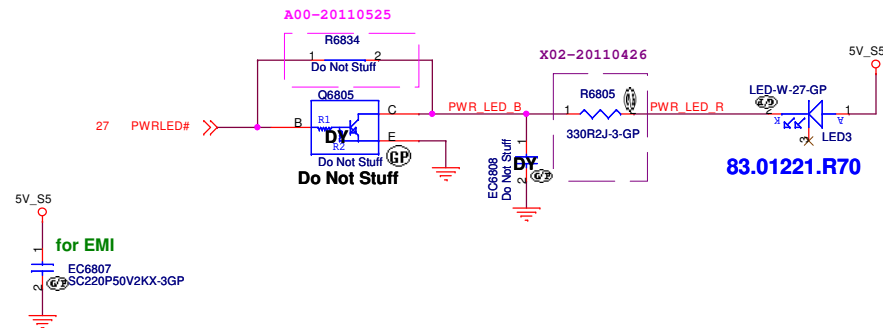


SSID = User.Interface

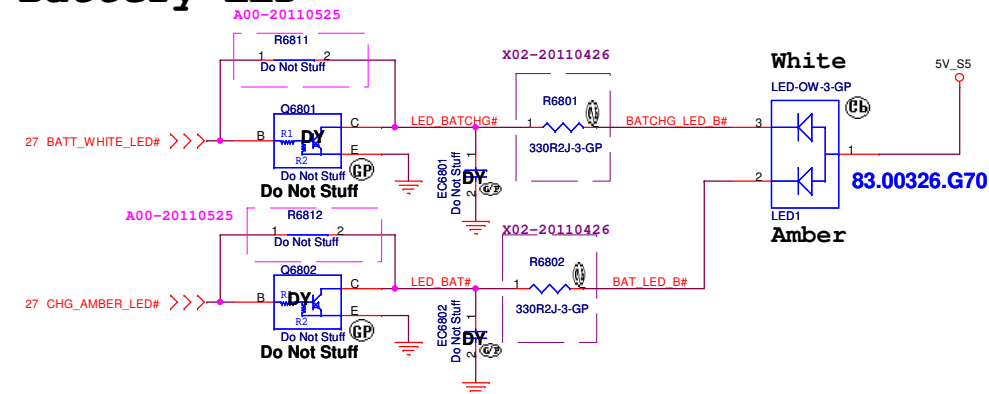
## Power BTN Connector



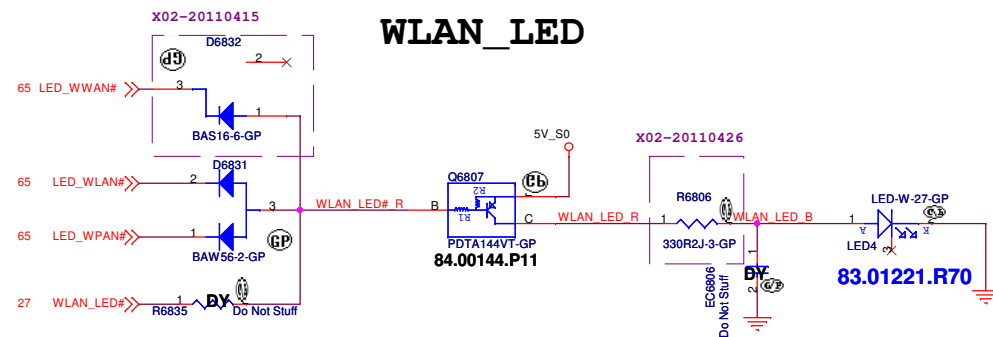
## Power LED



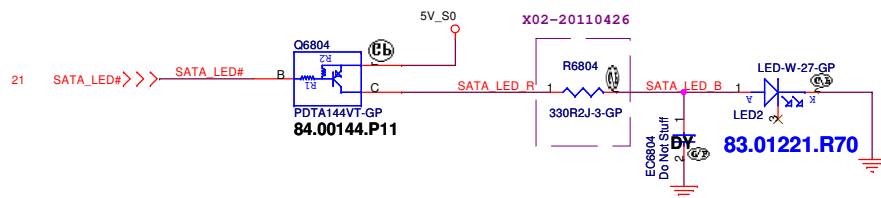
## Battery LED



## WLAN\_LED



## HDD LED



LED Location from left to right  
(MB, Top View)

LED3 PWR    LED2 HDD    LED1 Battery    LED4 Wifi

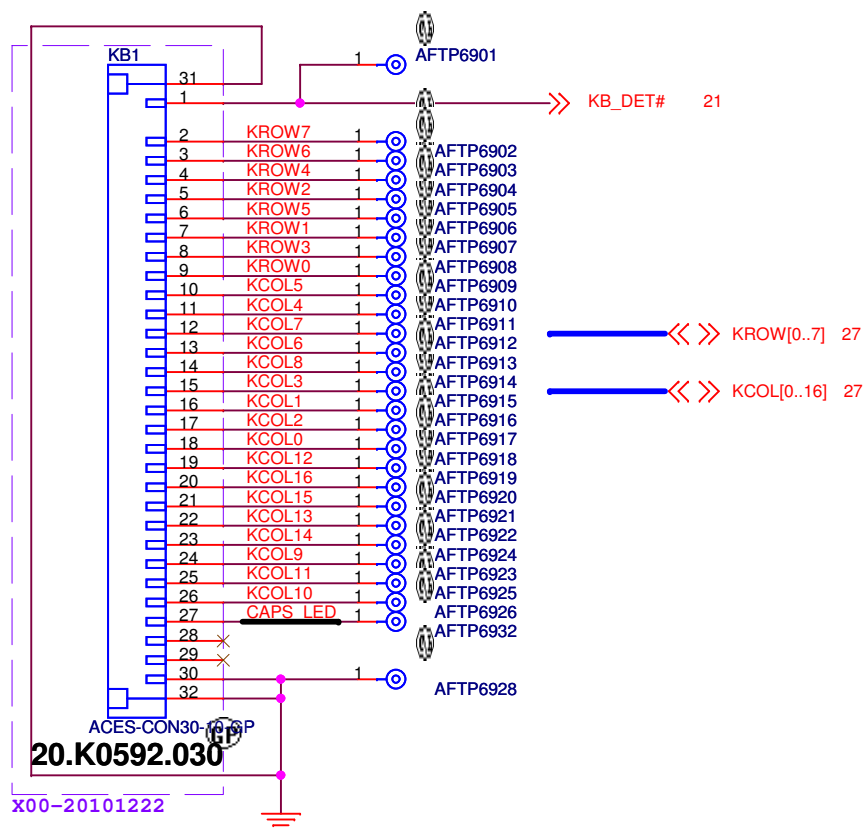
DV15 HR Vos GIGA HDMI NoSurge



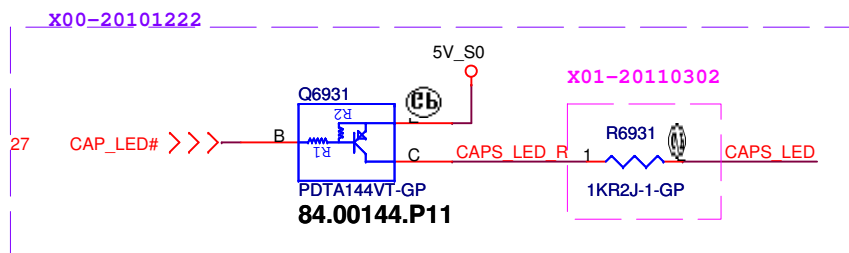
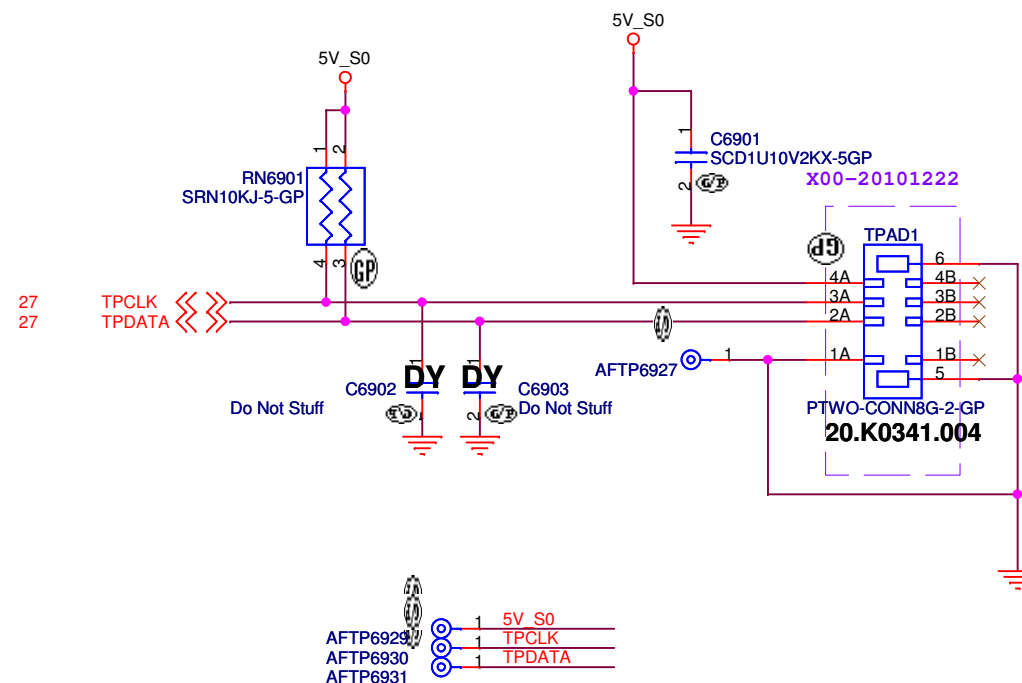
Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File			LED Bard/Power Button	
Size	Document Number	Enrico/Caruso 15 HR		Rev
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## Internal KeyBoard Connector



## TouchPad Connector



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Title

**Key Board/Touch Pad**

Size

Document Number

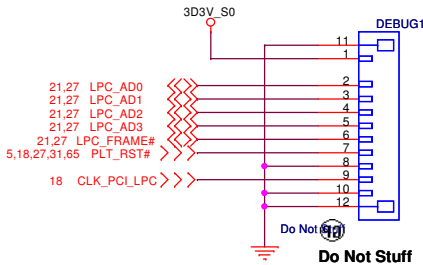
Rev

**Enrico/Caruso 15 HR**

**X01**

Date: Thursday, June 02, 2011

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DV15 HR Vos GIGA HDMI NoSurge

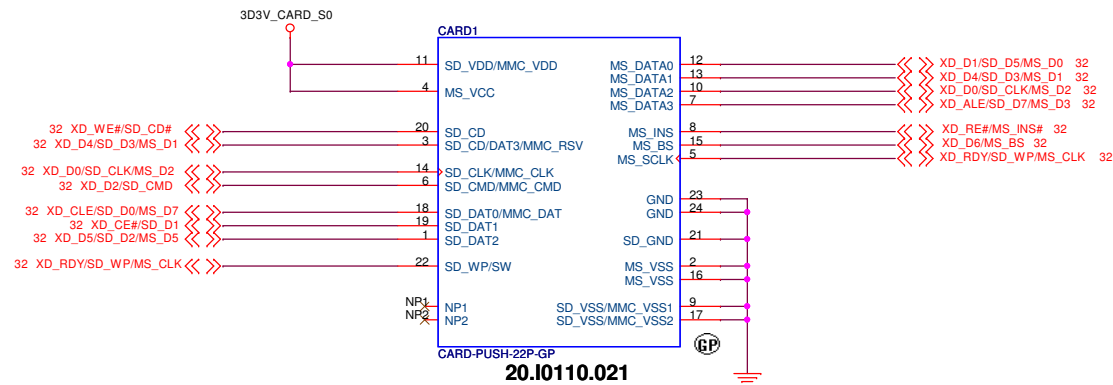
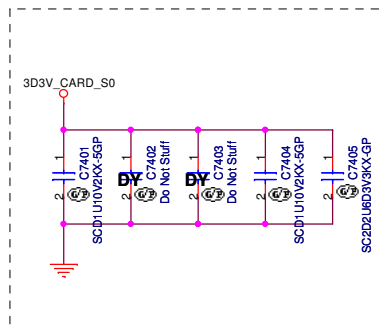


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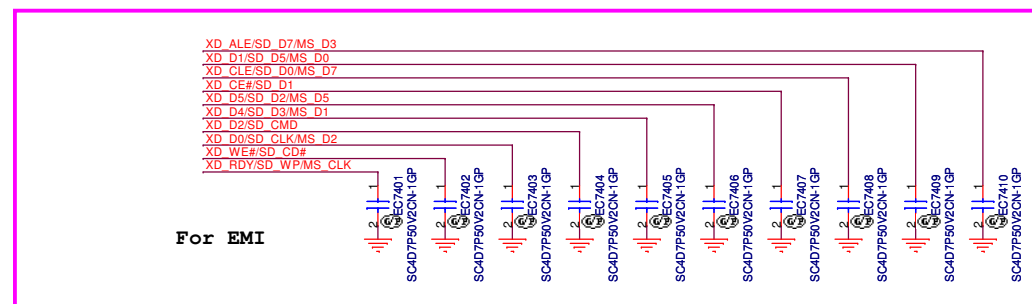
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Size	Document Number			Rev
A3		<b>Enrico/Caruso 15 HR</b>		<b>X01</b>
Date: Thursday, June 02, 2011		Sheet	71	of 104

SSID = SDIO

## SD/MMC/MS Card Reader



X01-20110315

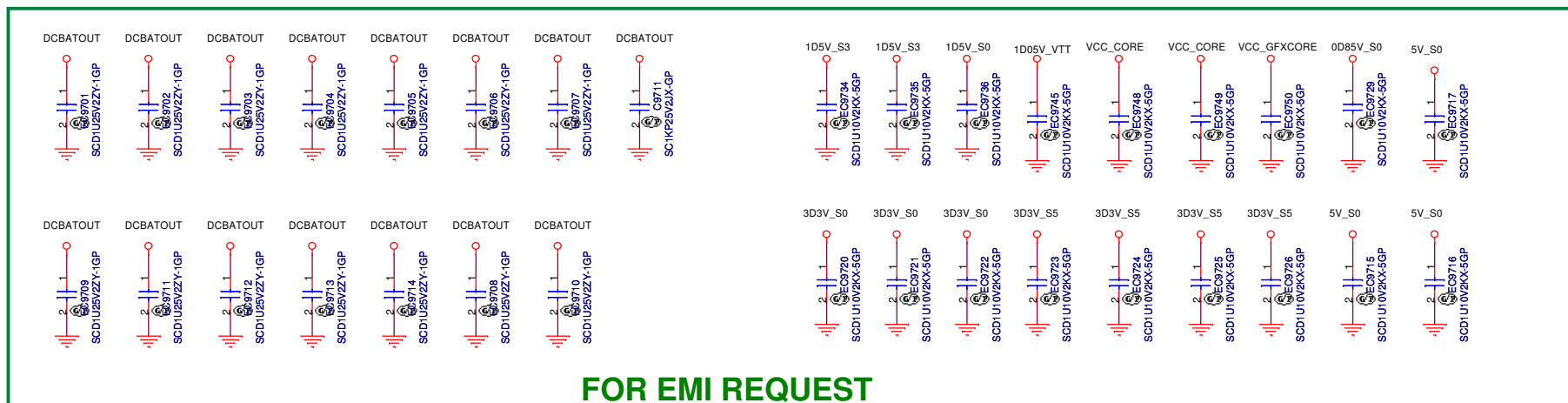
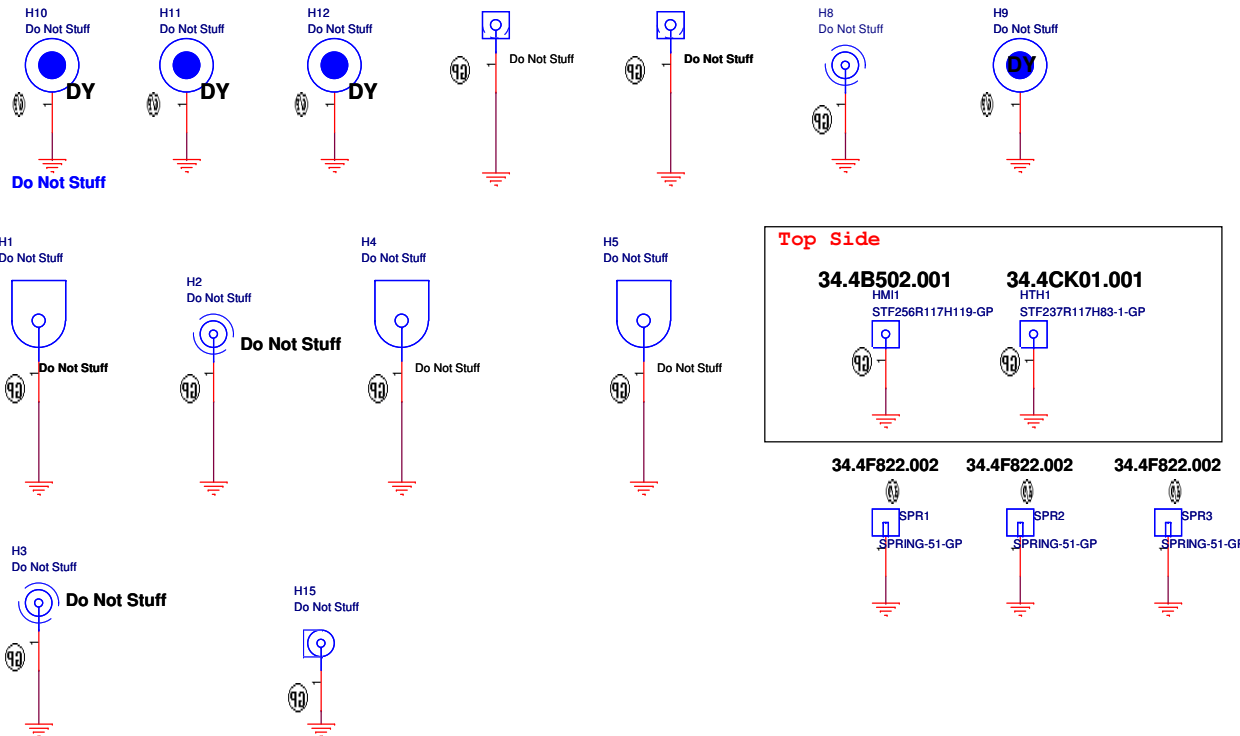


DV15 HR Vos GIGA HDMI NoSurge



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Title		
<b>SD/MS/MMC Card CONN</b>		
Size	Document Number	Rev
A3	<b>Enrico/Caruso 15 HR</b>	<b>X01</b>
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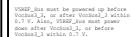


red word: KBC GPIO



0 This signal represents the Power  
Good for all the non-CORE and  
non-practice power rails.

red word: KBC GPIO



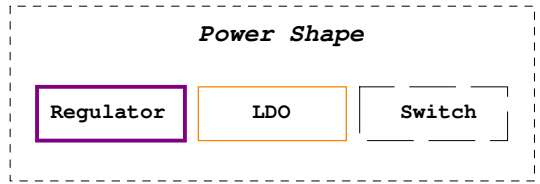
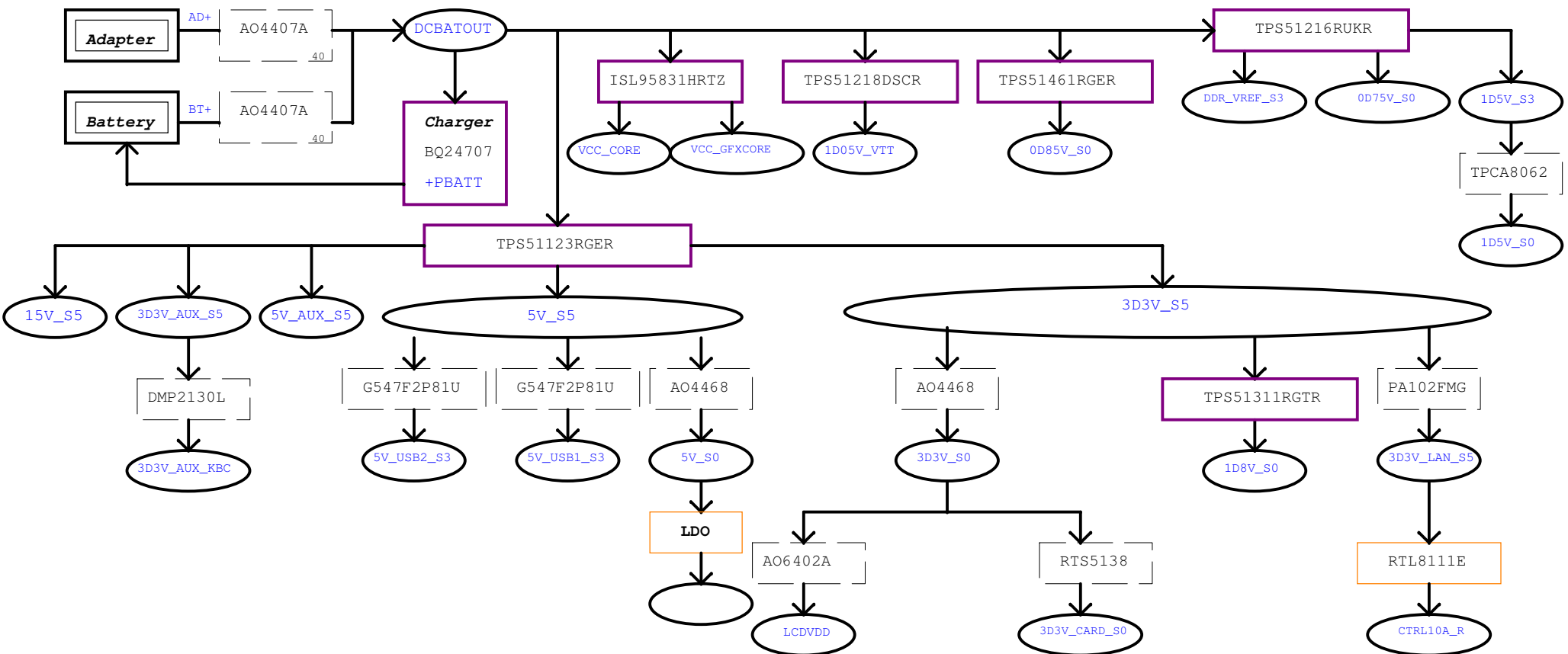
VIAREF must be powered up before Vcc1\_3, or after Vcc1\_3 within 0.7 V. Also, VIAREF must power down after Vcc1\_3, or before Vcc1\_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.

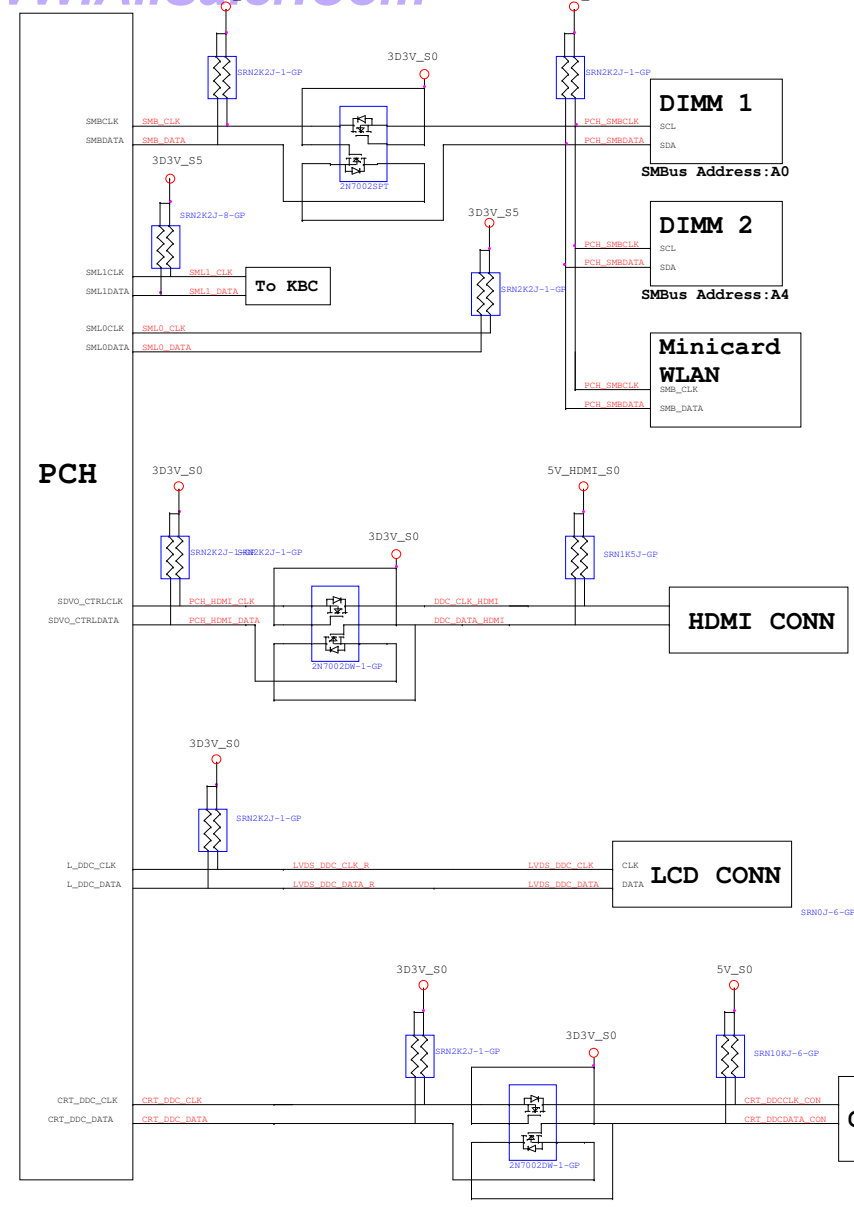


Power Up Sequence:  $-8 \sim 15$

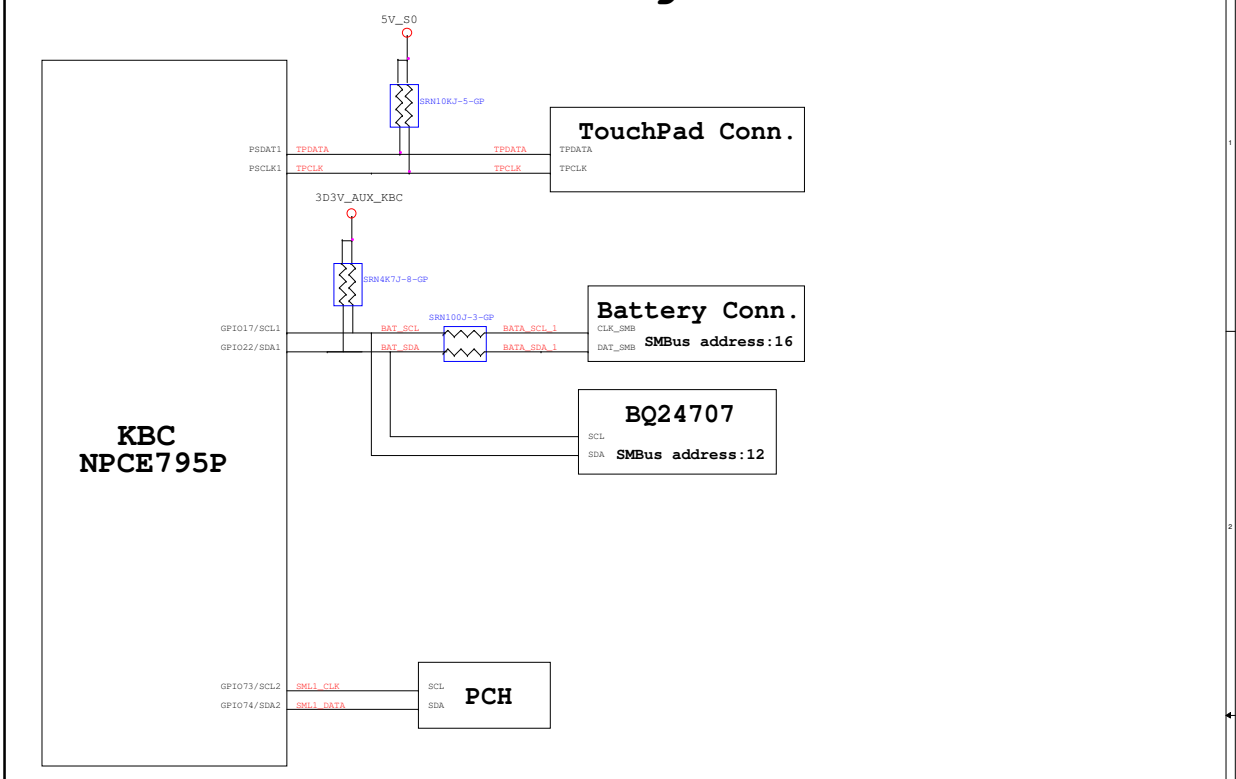


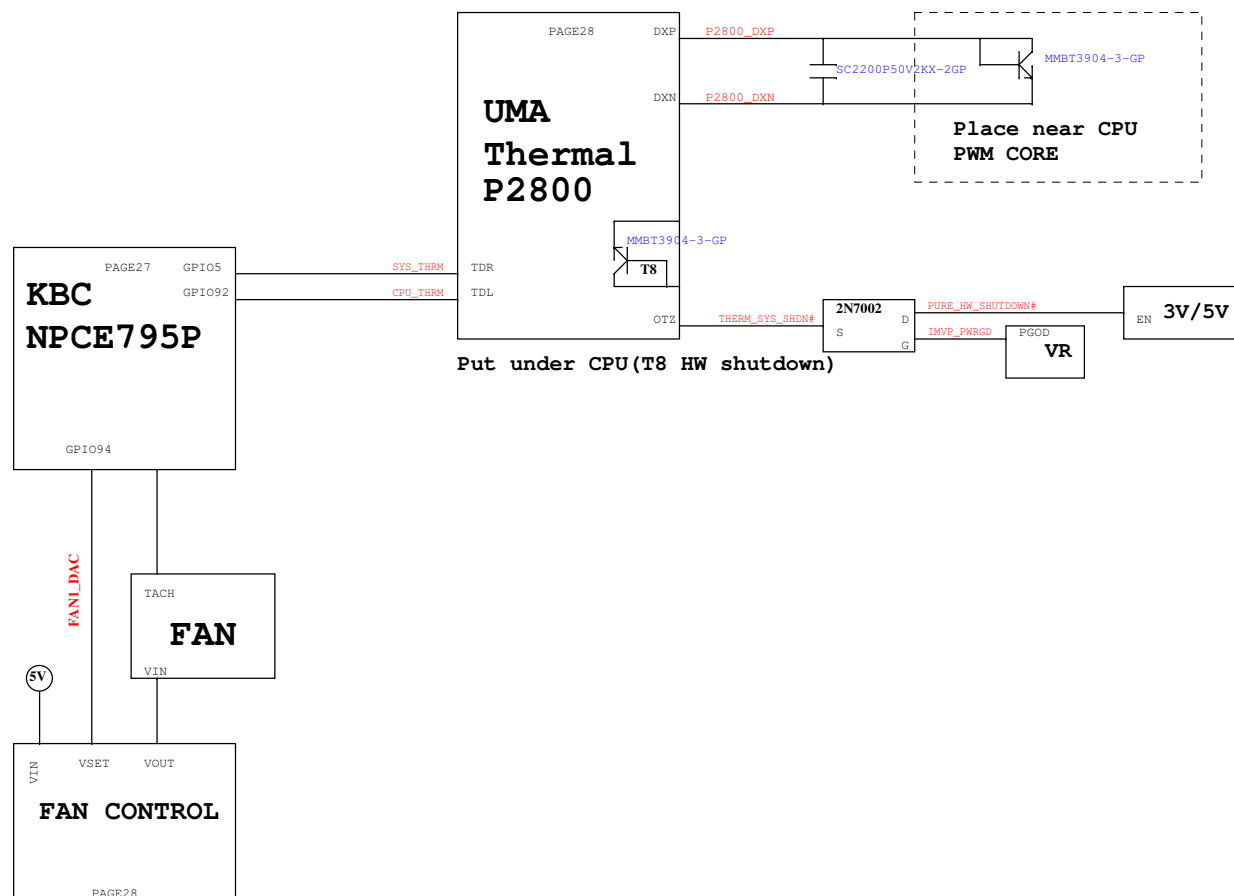


PCH SMBus Block Diagram



KBC SMBus Block Diagram





The diagram shows the pinout for the 92HD87B3 Codec. The pins are organized into four groups, each connected to a specific external component:

- SPEAKER:** Connected to SPKR\_PORT\_D\_L- and SPKR\_PORT\_D\_R+.
- HP OUT:** Connected to HP1\_PORT\_B\_L and HP1\_PORT\_B\_R.
- MIC IN:** Connected to HP0\_PORT\_A\_L, HP0\_PORT\_A\_R, and VREFOUT\_A\_OR\_F.
- Analog MIC:** Connected to PORTC\_L, PORTC\_R, and VREFOUT\_C.

Pin	Signal	Component
SPKR_PORT_D_L-	SPKR_PORT_D_L-	SPEAKER
SPKR_PORT_D_R+	SPKR_PORT_D_R+	
HP1_PORT_B_L	HP1_PORT_B_L	HP OUT
HP1_PORT_B_R	HP1_PORT_B_R	
HP0_PORT_A_L	HP0_PORT_A_L	MIC IN
HP0_PORT_A_R	HP0_PORT_A_R	
VREFOUT_A_OR_F	VREFOUT_A_OR_F	
PORTC_L	PORTC_L	Analog MIC
PORTC_R	PORTC_R	
VREFOUT_C	VREFOUT_C	



[illegible][illegible]

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Title	Author	Year	Journal	Volume	Page
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### Change History

Size	A3
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Document Number	
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**Enrico/Caruso 15 HR**

Rev

**X01**